FPGA based readout and preprocessing system for tomographic data

Karol Farbaniec, Jagiellonian University, Kraków

Introduction

In recent years rapid increase of resources in programmable systems arises from technological improvements in semiconductor industry.

That brings step towards moving software algorithms implementation in to hardware. That is why high throughput, streaming applications and data acquisition systems nowadays are often powered by FPGAs.

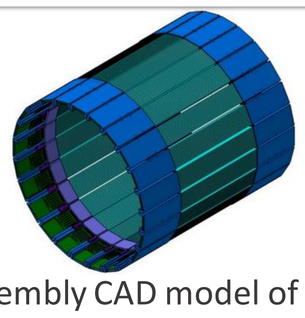

Figure 1. Assembly CAD model of Digital J-PET

Digital J-PET scanner leads innvation in Positron Emission Tomography.
Modular, low cost device with customizable imaging methods dedicated for medical applications possibly will facilitate conducting experiments in particle physics related topics.

System design

Overall approach

Based on J-PET DAQ design[1]

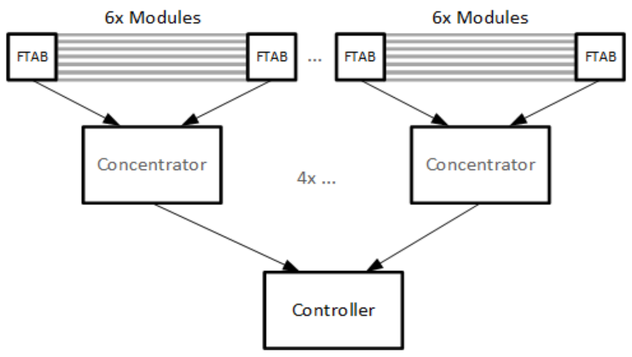

Figure 2. Digital J-PET DAQ conceptual scheme

Evaluation milestone

Module-wise processing geometry independent

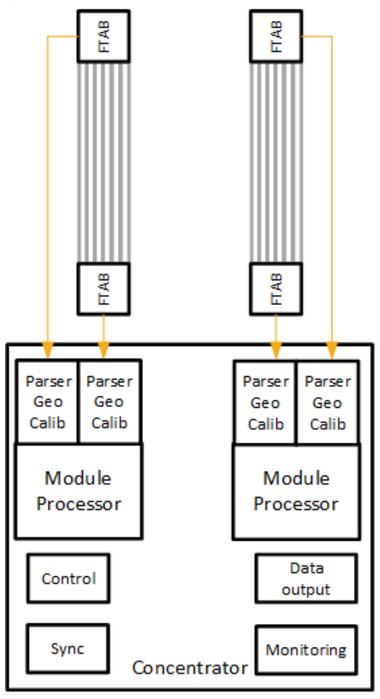

Figure 3. Perpendicular two module setup scheme

Data pipeline

Packets datapath

- Clock-domain-crossing from transmission to processing
- Parsing packet header, calibration, coincidence matching
  - Results in radiation receival position in module
- Scanner geometry mapping
  - Brings about raw source position
    - Line of response - LOR
    - Region of response - ROR

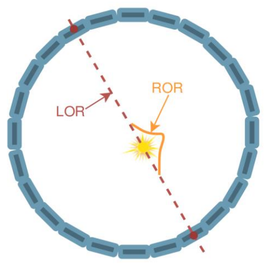

Figure 4.
LOR and ROR scheme

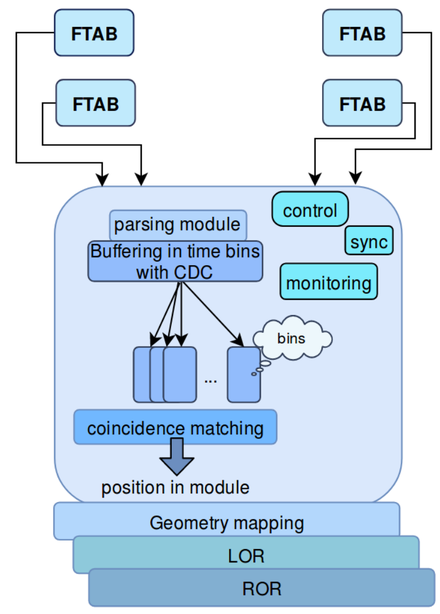

Figure 5.
Datapath conceptual diagram

Forwarding data to top level device

Depending on assembled experimental setup preprocessed data is forwarded to top level device(s) (for overall approach controller board with user interfaces). Then it is ready for high level processing.

High level processing

Controller board & UI

Suitable MPSoC platform[2]:

- advancing HW accelerated application
- enabling custom user interface

Results and further development

Status

- Transmission: 5Gb/s, full duplex, data & control
- Data transmission synchronization:

Peak deviation of reconstructed clocks about 80ps

- Module-wise coincidence matching

Scaling up and resource utilization

Early findings from implementation stands for low resource utilization. It brings opportunity for optimizations in later steps of development and easy scaling up.

Next steps

- Raw data visualization (also called as naive)
- MPSoC HW/SW application prototype
- Moving imaging methods in to hardware
- Two perpendicular module evaluation setup

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fpga fais

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[1] G. Korcyl, P. Moskal, M. Kajetanowicz, M. Pałka, „A system for acquisition of tomographic measurement data", WO/2015/028594
[2] G. Korcyl, et al. J-PET Collaboration, „Evaluation of Single-Chip, Real-Time Tomographic Data Processing on FPGA–SoC Devices", IEEE Trans. On Med. Imaging, DOI: 10.1109/TMI.2018.2837741, May 2018

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