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Declarations under Rule 4.17:

- as to the identity of the inventor (Rule 4.17(i))
- as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))
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(54) Title: A METHOD AND A DEVICE FOR MEASURING PARAMETERS OF AN ANALOG SIGNAL

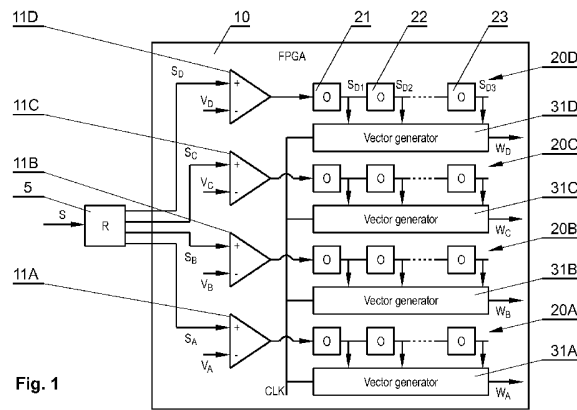


Fig. 1

(57) Abstract: A method for measuring parameters of an analog signal to determine times at which the analog signal (S) crosses predetermined voltage thresholds (VA, VB, VC, VD), the method comprising the steps of: splitting the analog signal (S) into a number of interim signals (SA, SB, SC, SD), the number of the interim signals corresponding to the number of the preset voltage thresholds (VA, VB, VC, VD); providing an FPGA system (10) comprising differential buffers (11 A, 11 B, 11 C, 11 D) with outputs connected to a number of sequences (20A, 20B, 20C, 20D) of delay elements (21, 22, 23), the number of sequences of delay elements corresponding to the number of the preset voltage thresholds (VA, VB, VC, VD); inputting, to an input of each differential buffer (11 A, 11 B, 11 C, 11 D), one interim signal (SA, SB, SC, SD) and a reference voltage corresponding to a particular preset voltage threshold (VA, VB, VC, VD); reading, by means of vector generators (31 A, 31 B, 31 C, 31 D), assigned separately to each of the sequences (20A, 20B, 20C, 20D) and connected to a common clock signal (CLK), current values of output signals of each of the delay elements (21, 22, 23) in the particular sequence (20A, 20B, 20C, 20D) at the same moment for all vector generators and providing these values as sequence output vectors (WA, WB, WC, WD); and determining times at which the analog signal (S) crosses the predetermined voltage thresholds (VA, VB, VC, VD) on the basis of the values of the sequence output vectors (WA, WB, WC, WD) and the delays introduced by the delay elements (21, 22, 23).

