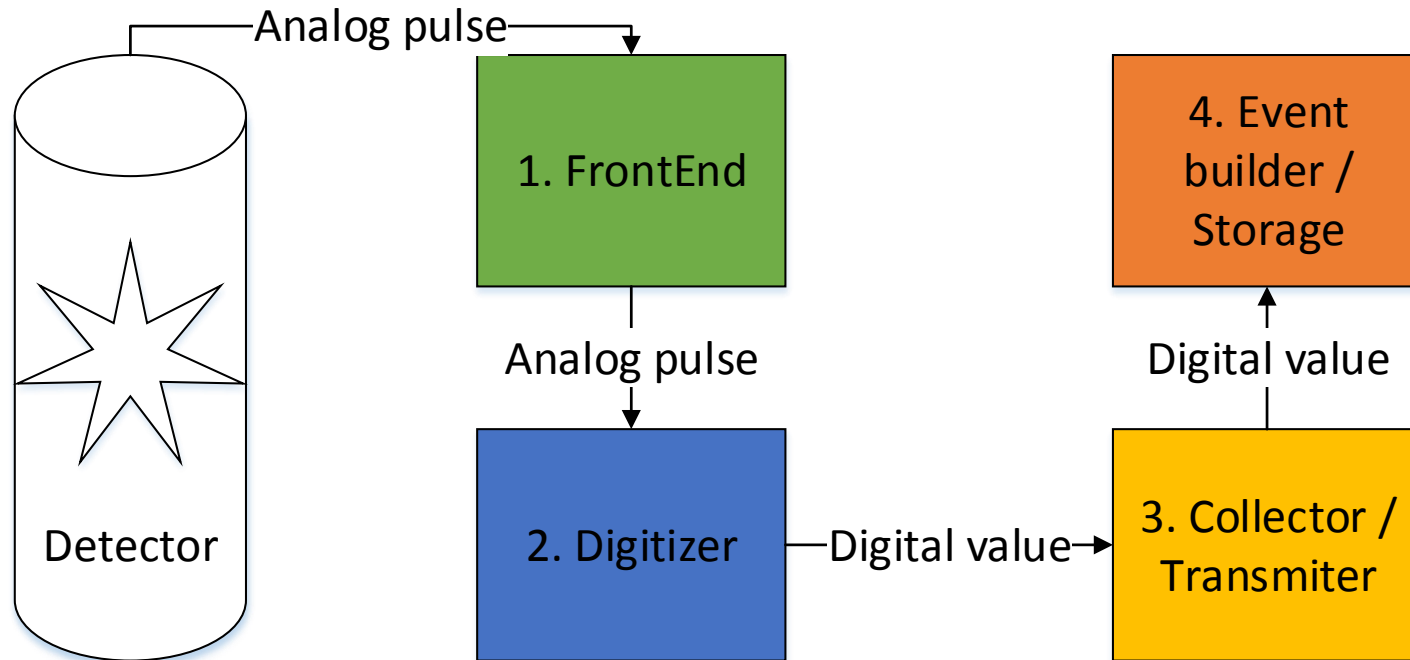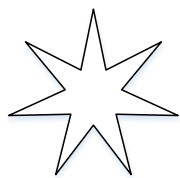# SAMPLING FEE AND TRIGGERLESS DAQ FOR THE J-PET SCANNER
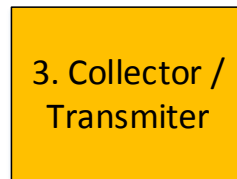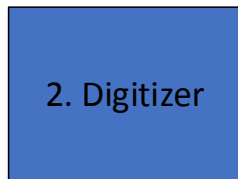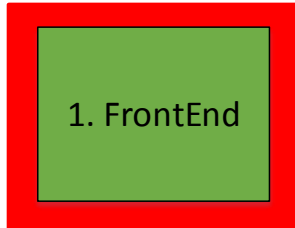
Grzegorz Korcyl, Jagiellonian University 2015

Outline

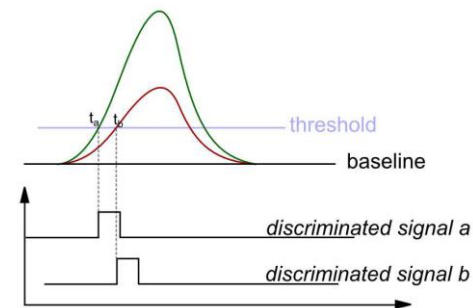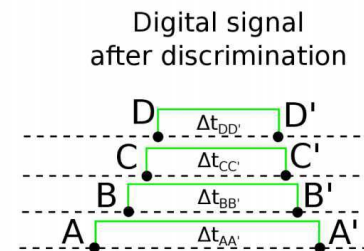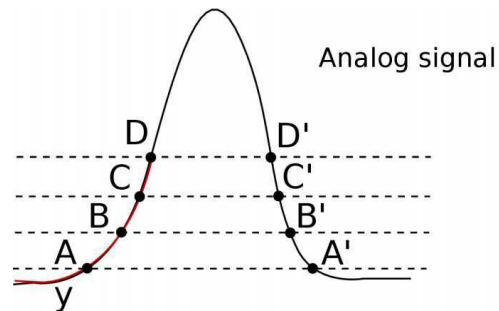- Input analog signals:
  - Sharp edges < 2ns
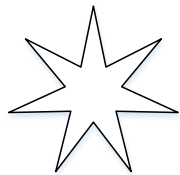 - Amplitudes < 1V
- What do we need:
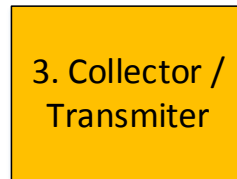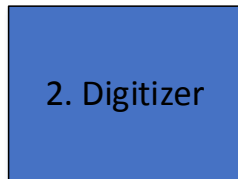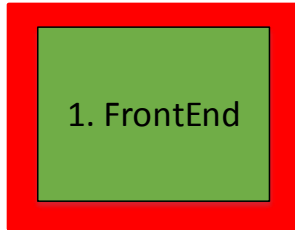 - Precise signal start time (time walk effect)
  - Time Over Threshold

- Multi-Voltage Threshold discrimination
  - Passive input signal splitter
  - Fast amplifiers
  - Programmable DACs

- Discrimination technique:
  - Usage of LVDS buffers inside FPGA
    - Splitted signal on input A
    - Threshold voltage on input B
    - Logical output switching at levels crossing point
  - Discriminated signal already inside FPGA
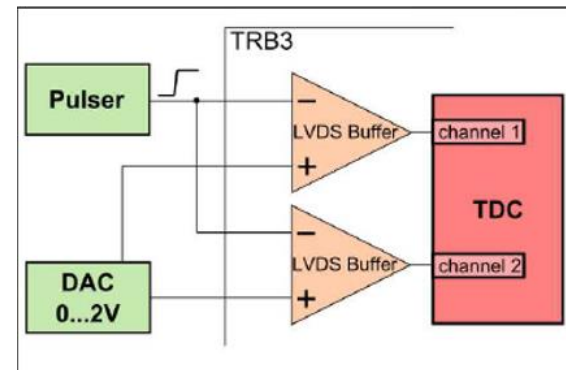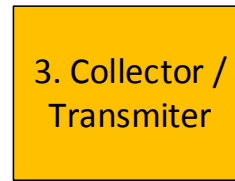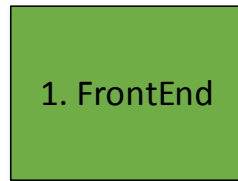
- JPET FEEv2
  - 16x input channels
  - 8x daisy chained DACs
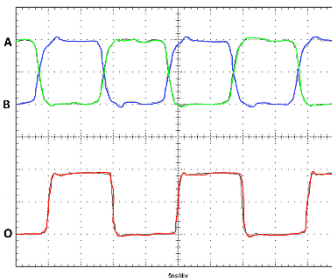
- Patent application [J-PET: M. Palka, et al.]
  - „A method and a device measuring parameters of an analog signal"
  - WIPO: WO/2015/028600, 2015

Detector	1. FrontEnd	2. Digitizer	3. Collector / Transmiter	4. Event builder / Storage
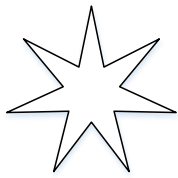
- ☐ High resolution TDC implementation inside FPGA
  - ☐ Discrimination and digitizer inside one chip
  - ☐ Time resolution 12ps
  - ☐ 48 channels with both edges per chip

- ☐ Achieved time resolution (PMT+FEE+TDC) < 100ps
  - ☐ Time difference between two PMTs on the same strip

σ =111 ps

σ =95 ps

Counts

Offline Corrections OFF

Offline Corrections ON

Time difference [ps]
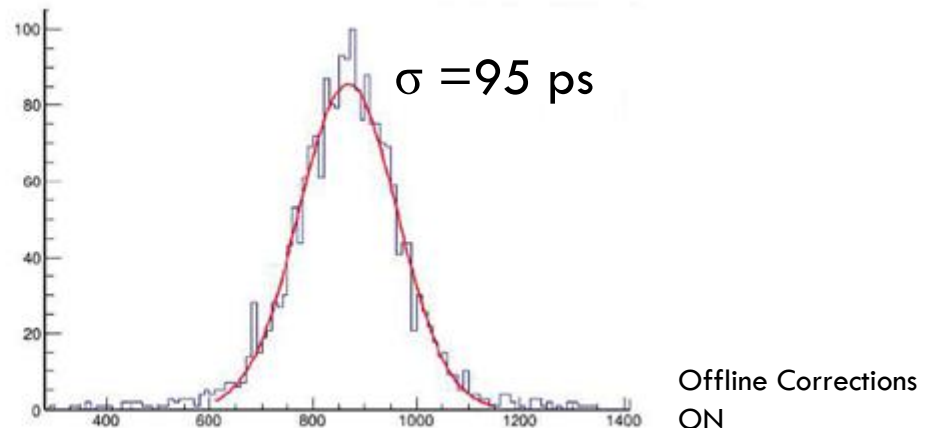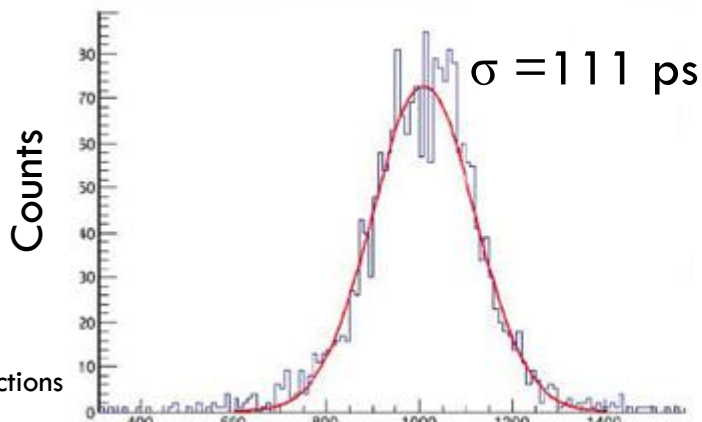
Detector | 1. FrontEnd | 2. Digitizer | **3. Collector / Transmiter** | 4. Event builder / Storage
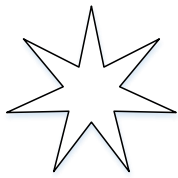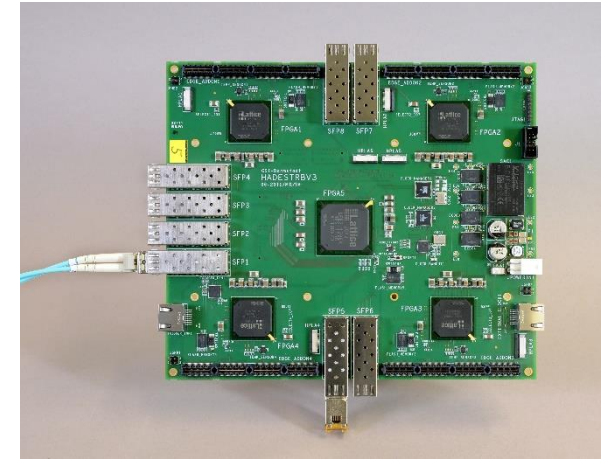
□ Trigger Readout Board v3 Platform

Korcyl, G.; Traxler, M.; Bayer, E.; Maier, L.; Michel, J.; Palka, M.
„A compact system for high precision time measurements (<14 ps RMS) and integrated acquisition for a large number of channels",
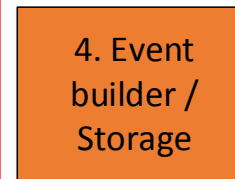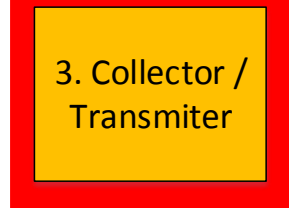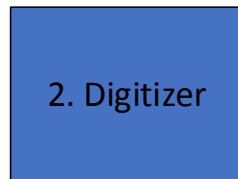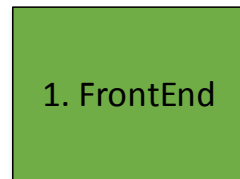JINST 10.1088/1748-0221/6/12/C12004

- ▫ 4x Edge FPGAs with TDC instances
    - ■ Connector for FEE (power, data, control)
- ▫ Central FPGA
    - ■ System controller
    - ■ Concentrator
    - ■ GbE Gateway
- ▫ Reconfigurable electronics
- ▫ Multiple boards connected in master-slaves mode
- ▫ Time synchronization through reference channels
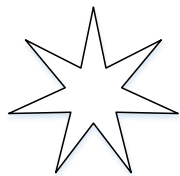
- Continuous data recording over the measurement period
  - Not used before in medical imaging scanners
  - 500 channels and data rates over 1GB/s
  - Constant 50kHz readout rate
  - Dead time reduced to minimum (order of tens ns)

- Pros:
  - No data loss due to preliminary event selection
  - Reduced measurement time
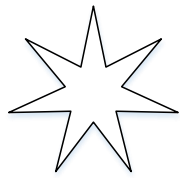

- Cons:
  - High data rates
  - Significant amount of storage, reaching up to TB per measurement
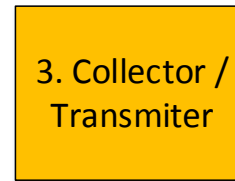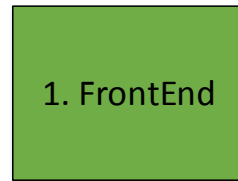 - A lot of background noise registered
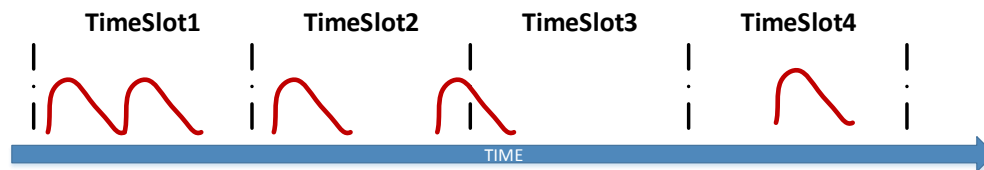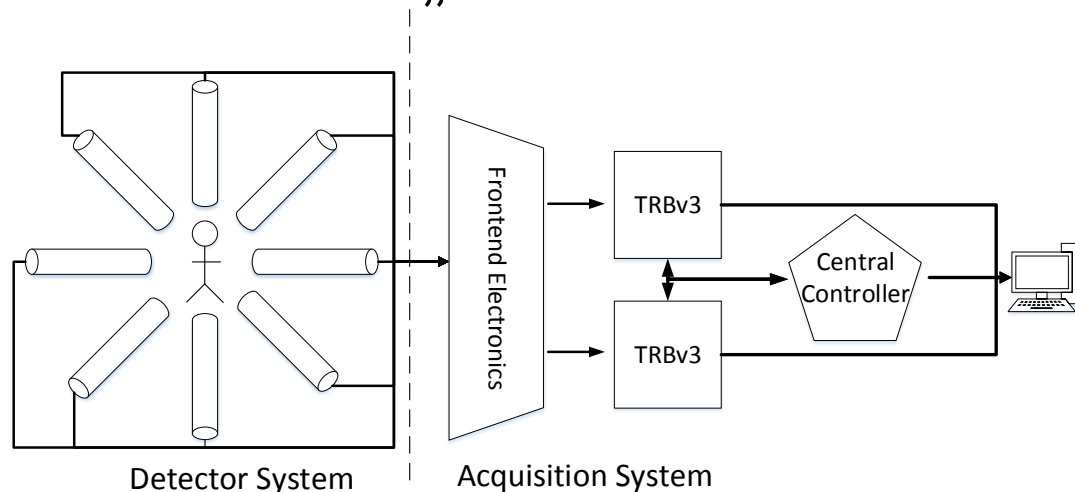
- Patent Application [J-PET: G. Korcyl et al.]
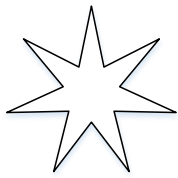 - „A System for acquisition of tomographic measurement data"
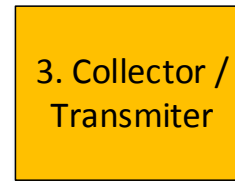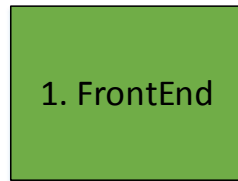 - WIPO/WO/2015/028594

□ Distribution of raw data over 16 machines

   □ Networking and storage issues

   □ Time consuming offline data filtering and preparation for analysis

□ Online filtering and event building

   □ Zynq SoC based board „in the middle"

Central Controller Module

- Hardware online processing of up to 16x GbE data streams

Firmware - RealTime   Software
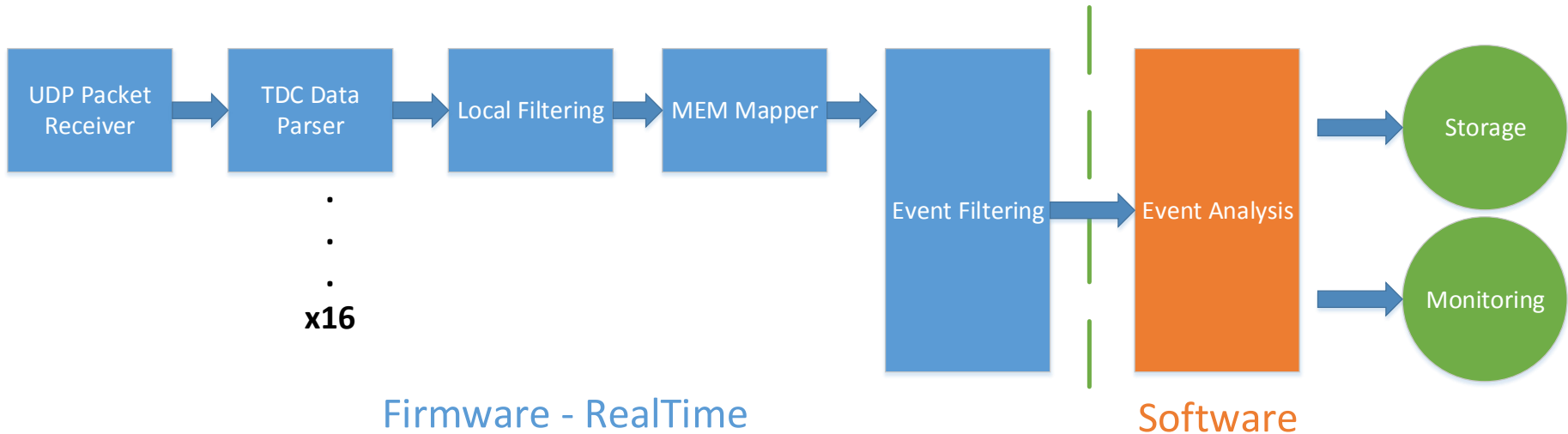
- Feature extraction on real time data streams
  - Data reduction
- High level software analysis
  - Online monitoring
  - High level data structures construction
  - Reconstruction algorithms

Summary

- A complete solution for signal measurement and data acquisition for JPET has been developed
  - Hardware
  - Firmware
  - Software

- Two novel methods:
  - Discrimination and time measurement as FPGA fabric and logic
  - Continuous readout mode

- Prototype setups constructed and under evaluation