FTAB - combining front-end, TDC and readout into small and compact board

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FTAB architectural requirements

- to cope with 13 photo multipliers sides
- each side of PM sources 4 SiPM signals, which gives in total 52 SiPM analogue signals
- two thresholds both for rising and falling edge of the signal
- measure time of signal arrival and its end, at the threshold level, with a very high precision < 40ps RMS
- compact design to place directly FTAB on the detector to avoid cumbersome cabling
- low power consumption to avoid heating boards surrounding
- low voltage ripple on the power supply
- read-out large amount of measurements data downstream to the data merger

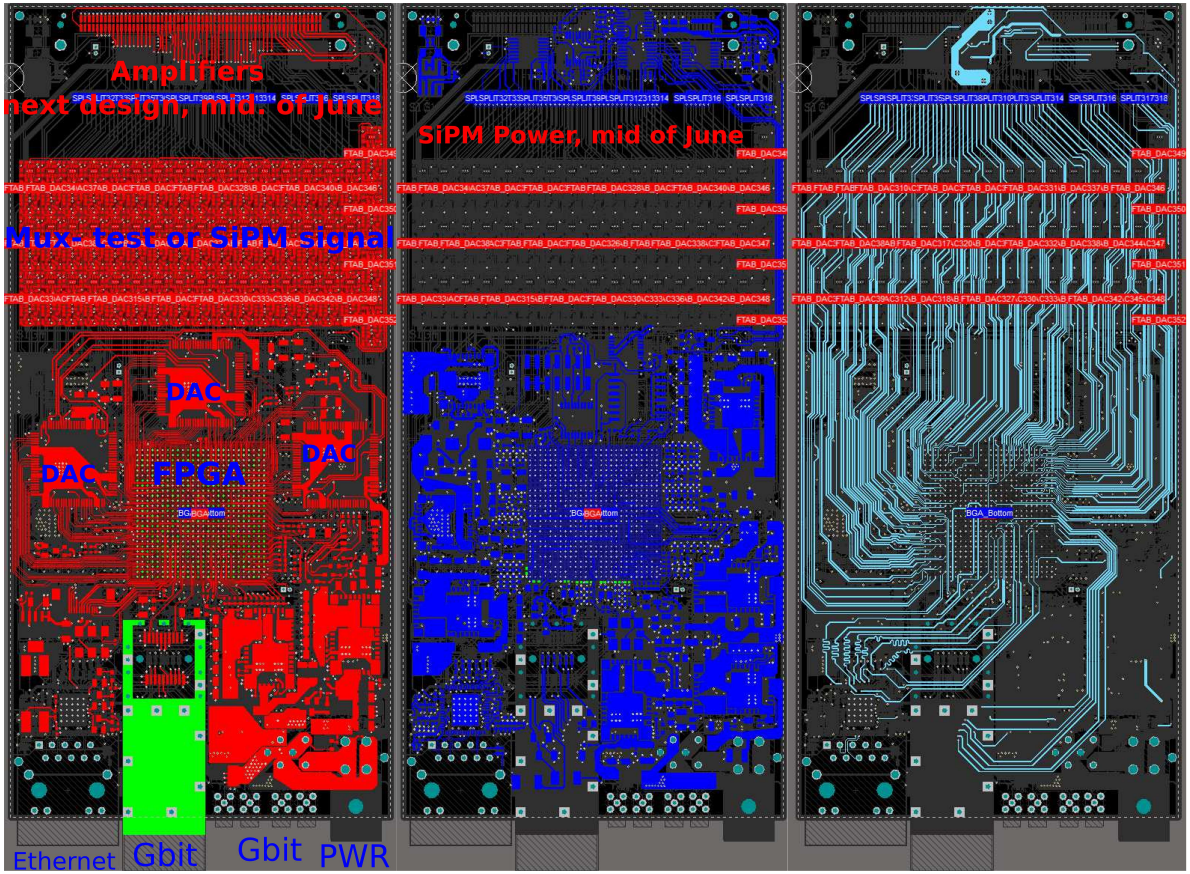


Fig. 1: FTAB PCB layers, on the left top layer, in the middle bottom and on the right one of the middle layers

PCB characteristics

- 1787 used components
- 34377 tracks between components
- 3134 vias
- only 16 × 7cm size
- 8 layers
- width and thickness of crucial paths are assuring lower cross-talk effects
- track for SiPM signals have 50Ohm impedance (carefully checked with manufacturer)

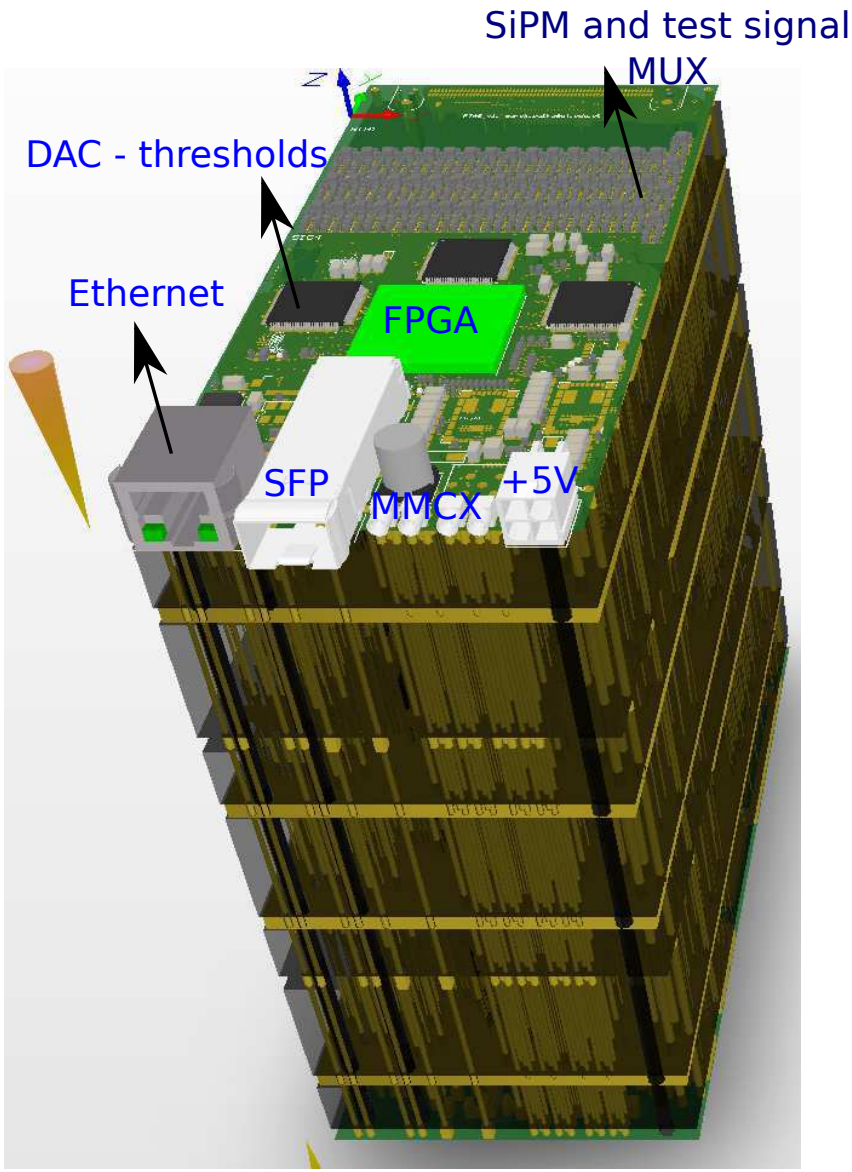


Fig. 2: 3D view of the FTAB board with marked components

Equipped components

- negative SiPM signals are adapted to be used by FPGA differential buffers
- the central place is taken by Artix7 200T FPGA
- FPGAs differential buffers are used as comparators, speed grade is -2
- three DACs are 12 bit precision, 40 channels, Analog Devices chips AD5381
- for connectivity purposes there are following interfaces:
  - Ethernet - foreseen to be used for stand alone operations
  - SFP is a 6 Gbit transmission line - readout plus control
  - MMCX connector - to chain up FTABs readouts
- on board DC/DC converters - 5V, 3.3V, 2.5V, 1.8V, 1.2V, two times 1.0V

- low ripple voltage well below Xilinx specifications, it assures low intrinsic noise for SiPM signals
- no problems with Gbit transmission at the maximum Artix7 rating
- stable DAC behaviour assured with careful schematics design
- level adapters low pass filter, reducing cross talk, fulfil its task
- all DAC are operational and deliver threshold voltages within AD5381 specifications
- FPGA core temperature is $\sim 70°C$ - when the whole firmware is running
- Ethernet has to be still tested

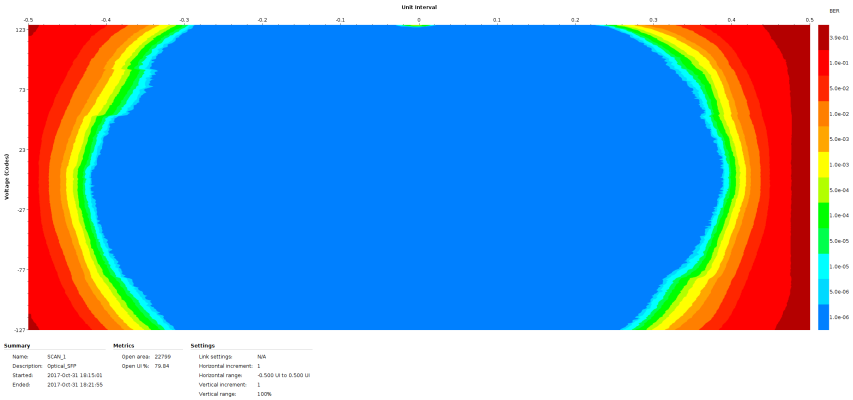


Fig. 3: Gbit transmission eye scan - very wide open area at 4Gbit/s shows very good transmission quality.

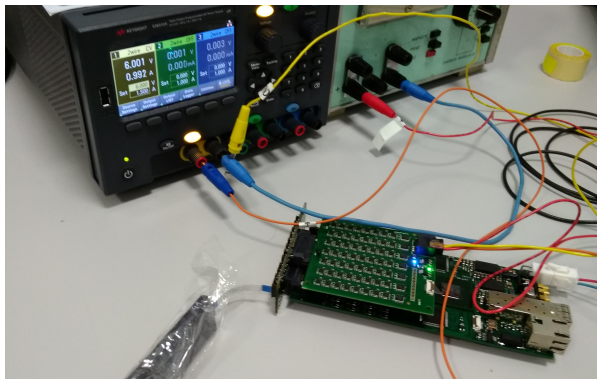


Fig. 4: One of the test setups connected with SiPM power supply board and amplification stage

- small form factor to fit into JPET modular design
- connected with SiPM power supply board and amplification stage
- amplification stage currently has 52 high frequency amplifiers
- amplifiers are proven to not heat up SiPM - measured temperature directly on the amplifier is on the level of $37^{o}C$
- active air flow induced by small fan is sufficient to keep SiPM in room temperature

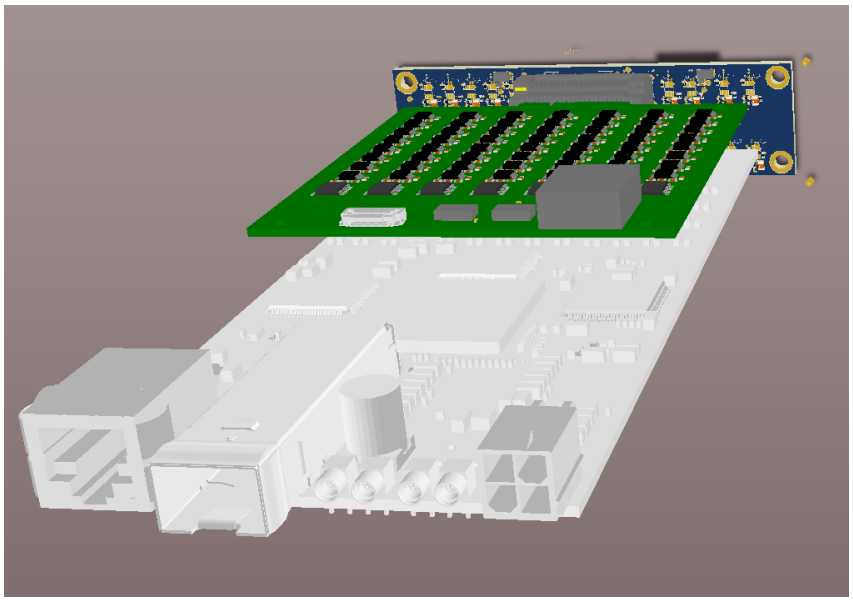


Fig. 5: 3D view of FTAB (grey) amplification stage (blue) and SiPM power supply (green) boards

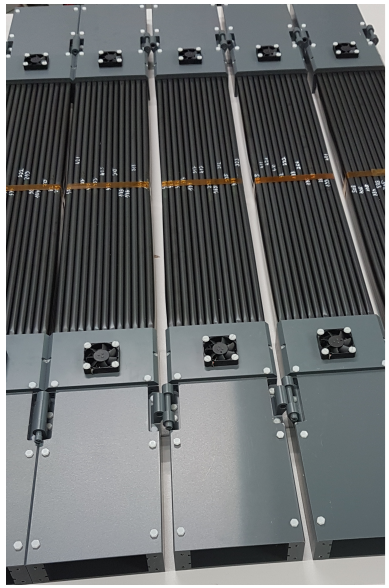
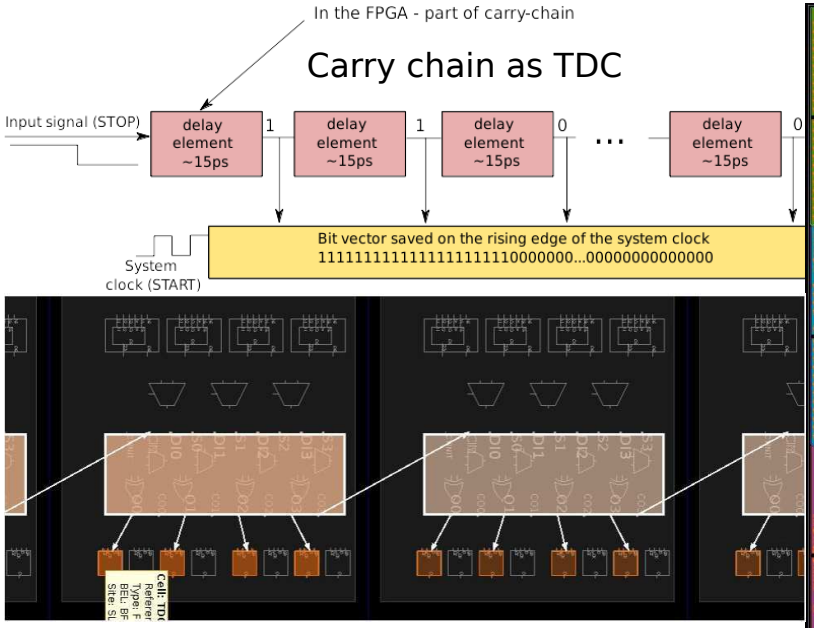
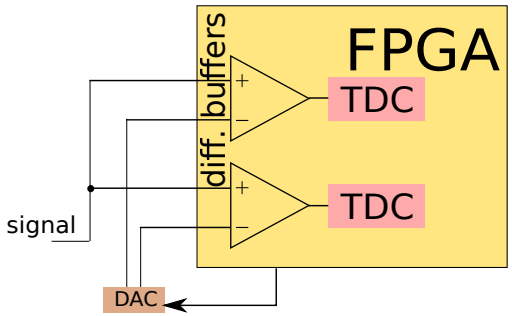


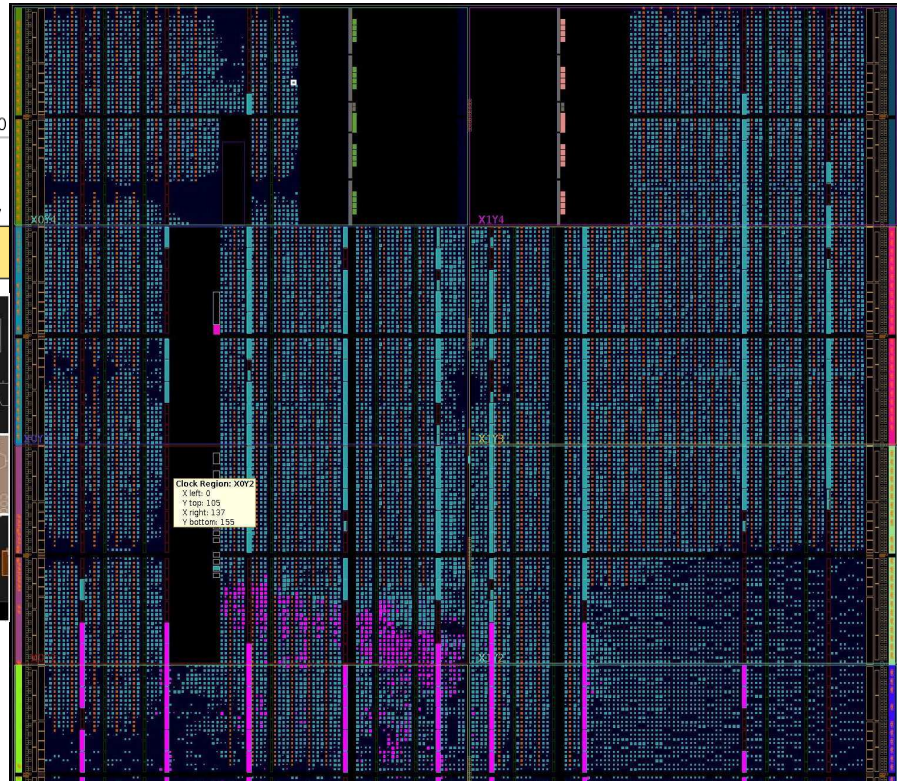
Fig. 6: JPET modules where front-end and read-out electronics is placed

Using FPGA both as a multi channel TDC and comparator device allows to significantly reduce size and cost.



Input buffer as comparator





FPGA - 104 channels implemented (space for more)
Firmware readout ready

Fig. 7: Implemented TDC have 30 ps RMS precision and they operate with 330MHz clock.

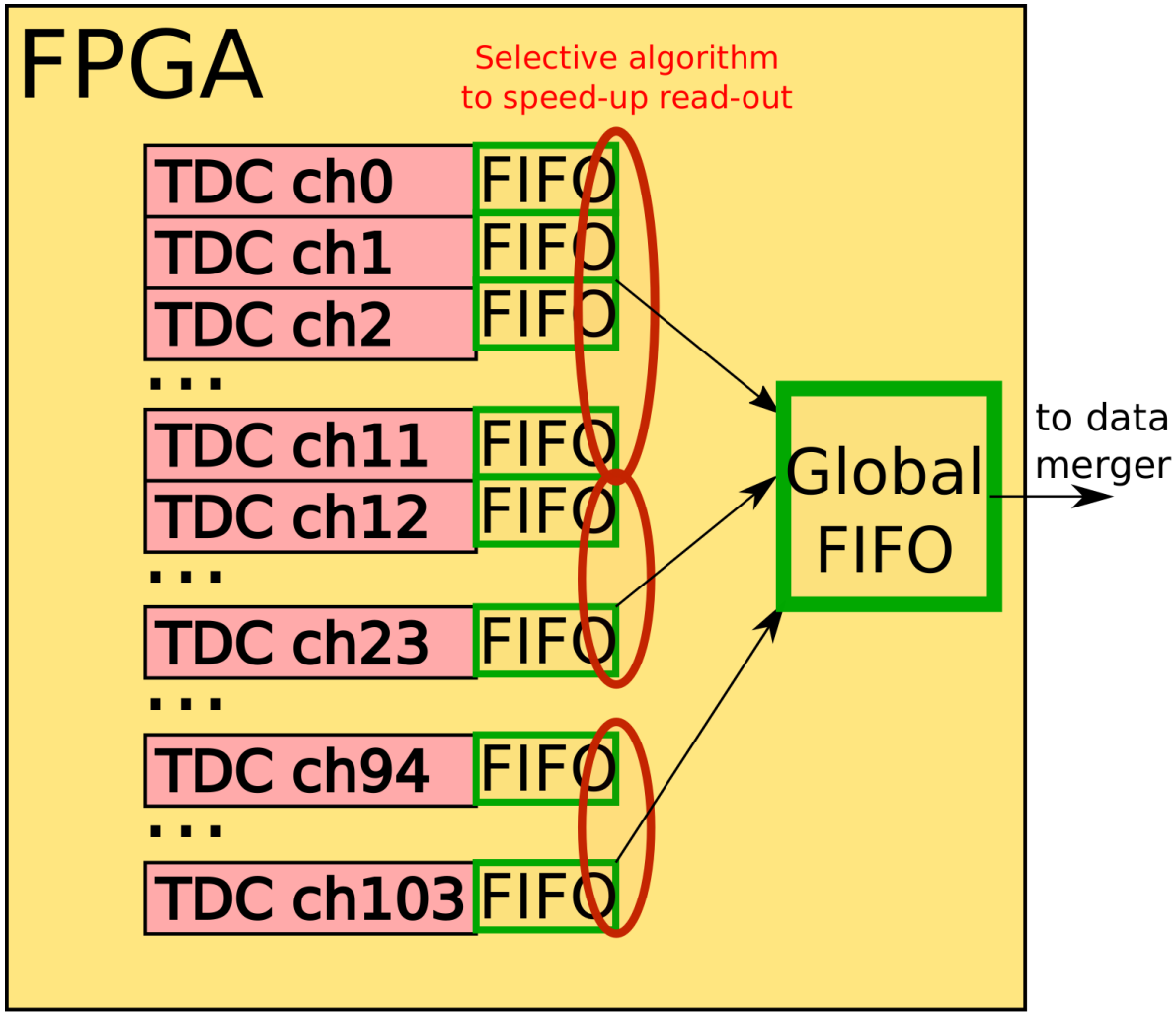


Fig. 8: Data is stored individaualy in TDC FIFOs. If one of the TDC FIFOs is not empty it is immiedietally read-out. To speed up read-out process fast algorithm is implemented (1 clock cycle) which gives list of pointers to not empty FIFOs. This significantly reduces dead time in read-out

Summary and Plans

- FTAB board fulfil all requirements to be used in the JPET
- majority of the firmware has been written
- FTAB will evolve to a board which will have **150** TDC/comparator channels
- next FTAB board will integrate amplification and power supply stage on one PCB with no significant changes to the board size
- final price per amplification/thresholding/TDC and readout channel will be ∼10 EUR