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FPGA BASED DATA ACQUISITION SYSTEMS FOR PHYSICS EXPERIMENTS

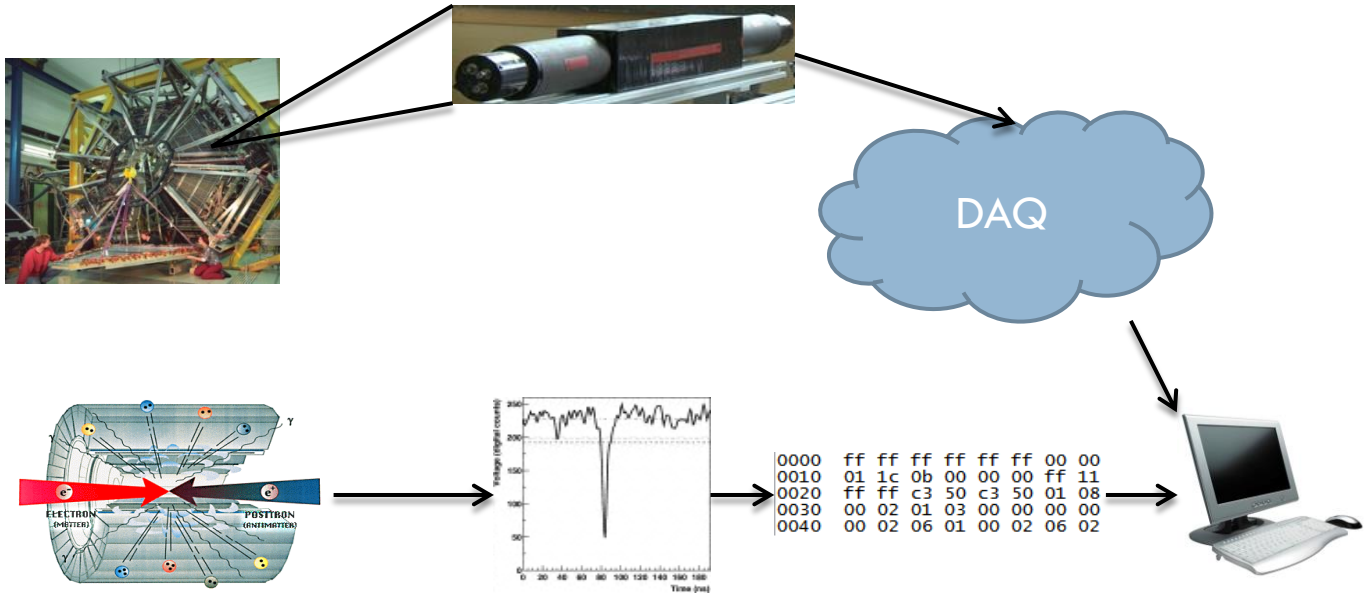
Grzegorz Korcyl – MPD symposium 2013

Outline

1. Data acquisition systems
2. Field Programmable Gate Arrays
3. FPGA based TDC
4. FPGA based TDC based ADC
5. Data collection and transmission
6. Perfect example - TRBv3
7. Main experiments
8. Summary

Data Acquisition Systems

- Hardware and software used to measure and digitalize analog signals generated by detectors



Data Acquisition Systems

- Readout – how to measure
  - Front end electronics
    - Prepare analog signals for measurement
  - Measurement devices
    - TDC – precise time measurement
    - ADC – analog signal sampling
      - Sampling ADC – signal shape recognition
      - QDC – collected charge
      - Peak detection
  - Readout electronics
  - Data collectors
  - Storage

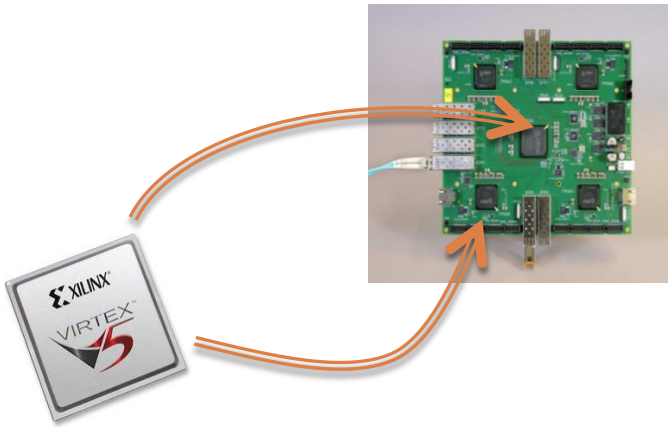
- Trigger system – when to measure
  - Signal distribution
  - Triggering levels

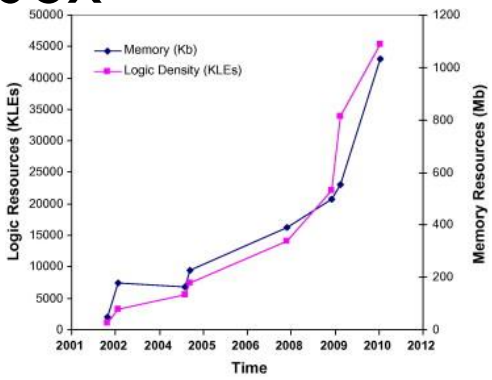
Data Acquisition Systems

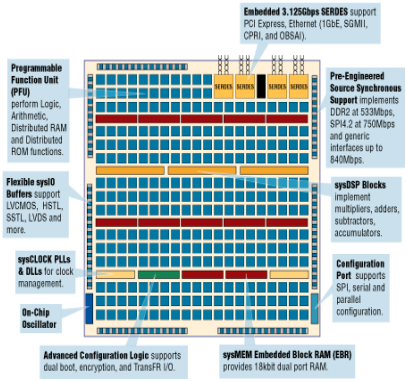
- Dedicated electronics
  - NIM/CAMAC/VME/ATCA modules
    - Pros:
      - Ready to use
      - Verified solutions
      - Interconnected
    - Cons:
      - Expensive
      - Closed solution
- Custom electronics
    - Pros:
      - Flexible solution
      - Easily expandable
      - Compact
    - Cons:
      - Workforce to develop the hardware
      - Workforce to develop the firmware for the hardware
      - Workforce to support

Field Programmable Gate Arrays

- Reprogrammable at any time
- Huge capacity
- Parallel processing
  - Different way of thinking
- Many hardware features ready out of the box
- Online data analysis
- System on chip





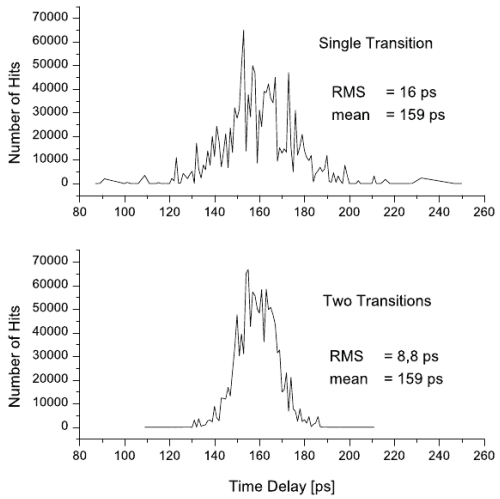


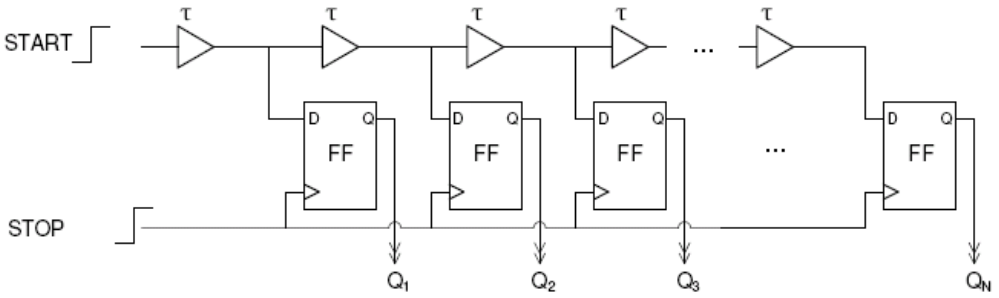
Field Programmable Gate Arrays

- Devices perfect for:
  - Digital data collection and transmission
    - Built-in memory and multi-gigabit transceivers
  - Parallel data processing
    - Built-in DSP blocks
    - Limited arithmetic operations
  - Slow control interface
  - Trigger logic implementation
  - Measurement device
    - FPGA based TDC
    - FPGA based TDC based ADC

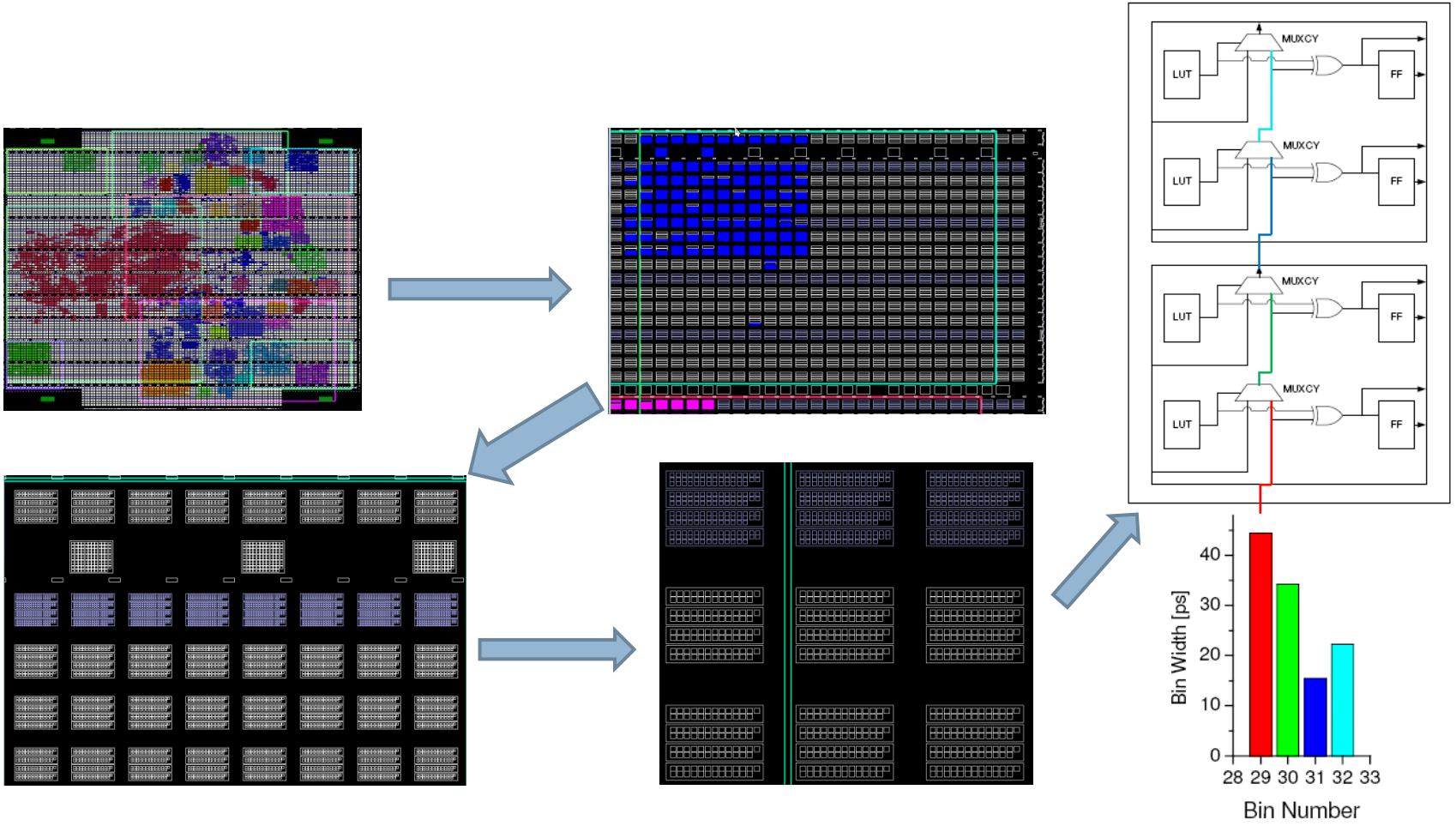
FPGA based TDC

- Use of the internal structure of the chip to create delay chains
- Highly configurable solution
  - Number of channels <-> single channel resolution
  - A lot of methods to improve resolution

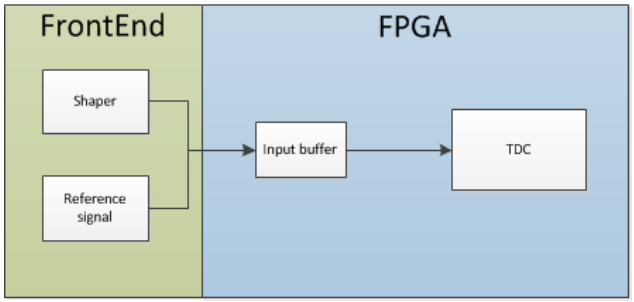




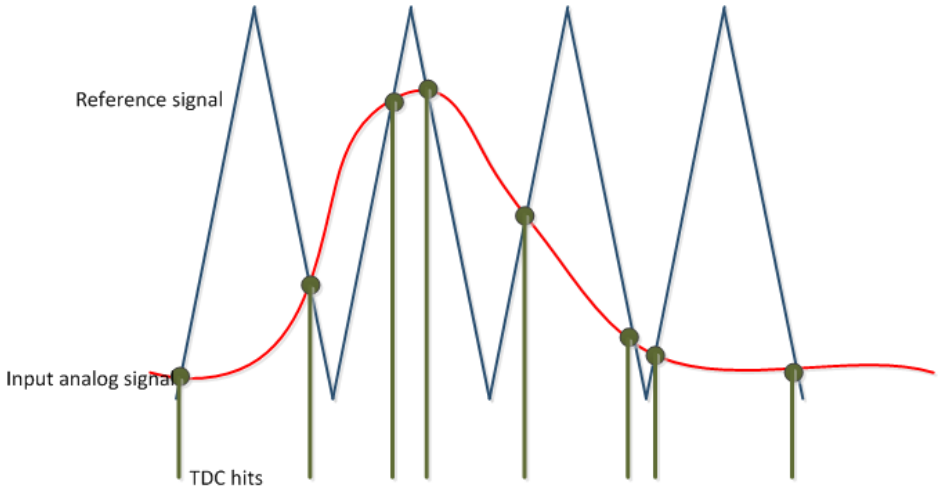
FPGA based TDC



FPGA based TDC based ADC

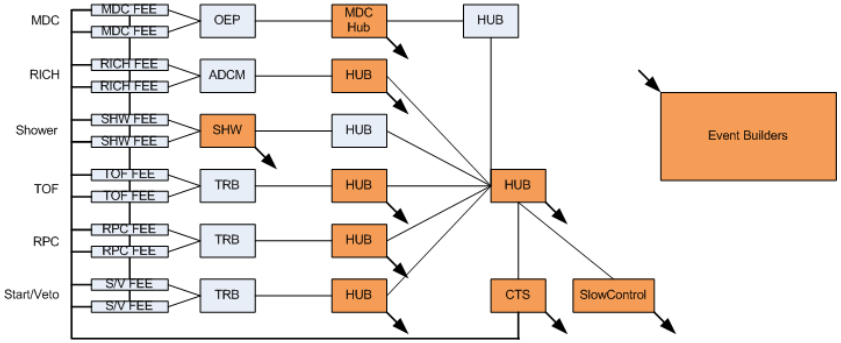


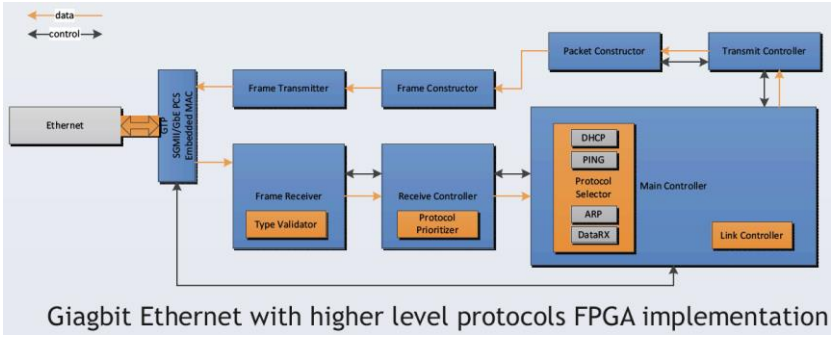
- Need of a very well defined
  and precise reference signal
- Input buffer generates a pulse
  when analog signal crosses reference signal
- The time of pulses is measured by built-in TDC
- Knowing the crossing time and
  the exact shape of ref signal
  one can calculate the sample
  values



Data collection and transmission

- FPGAs are equipped with many multi-gigabit transceivers
  - High speed connection to other electronics
  - Facilities for standard protocols implementations
    - Eg. Virtex7 96 – Full-Duplex transceivers, each 28,05Gbps
  - HADES: >500 interconnected boards with >1000 optical transceivers – 30 GbE

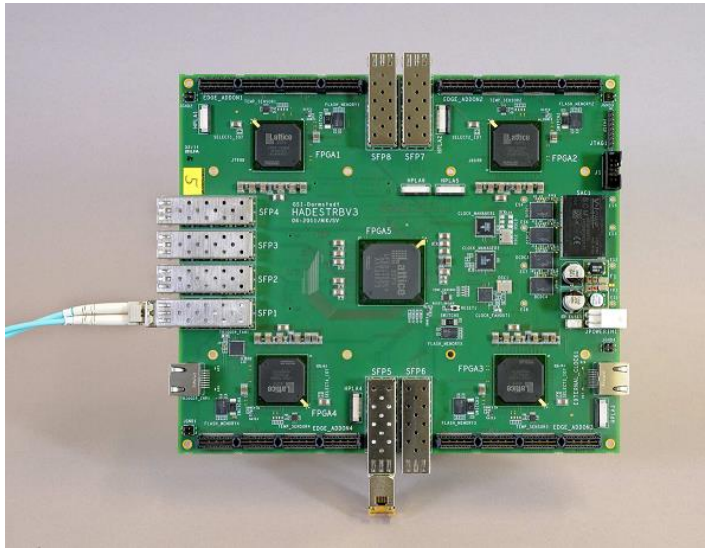




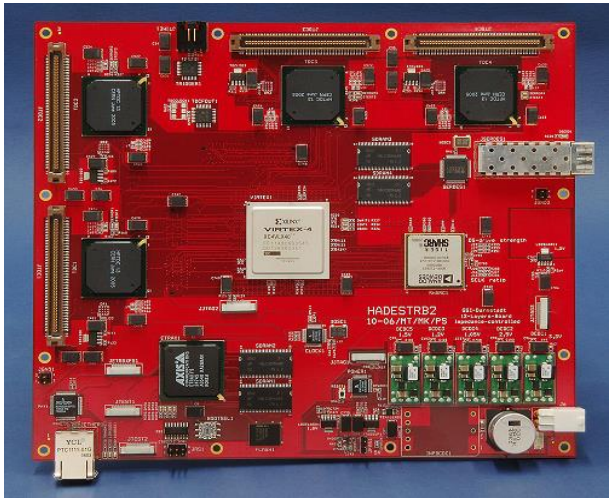
Giagbit Ethernet with higher level protocols FPGA implementation

Trigger Readout Board v3

- 5x Lattice ECP3 150 FPGAs
  - 4 edge devices
  - 1 central
  - Flash ROMs for each
- 8x 3.2Gbps optical links
- 4x 208pin QMS connectors
  - Small Addons
- 1x 106pin connector
  - Large Addon
- Hardware trigger input



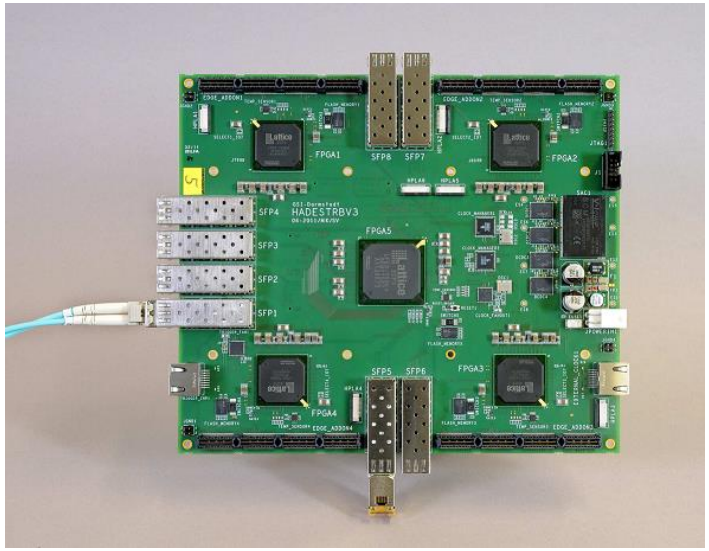
TRBv3



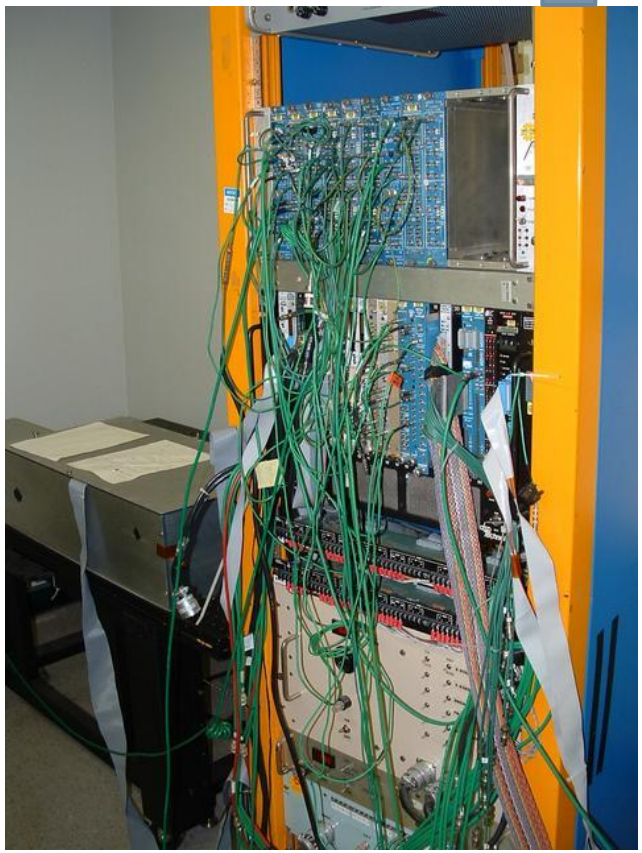
TRBv2

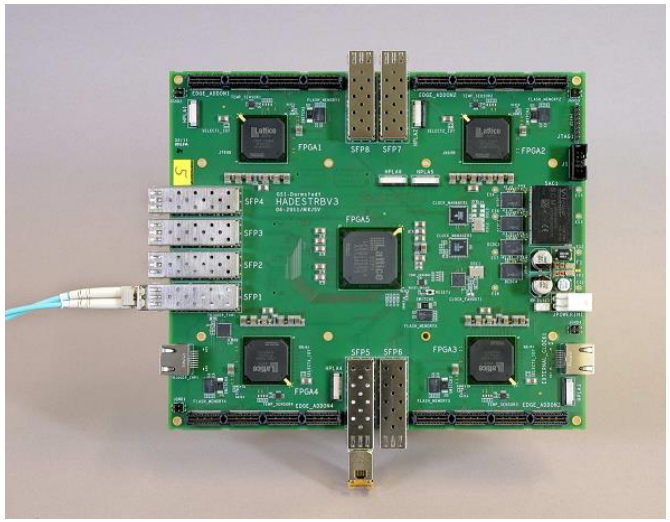
Trigger Readout Board v3

- Standalone measurement board
  - Central FPGA
    - Integrated trigger system
    - Integrated Slow Control
    - Readout of edge FPGAs
    - Data collection and transmission
  - Edge FPGA
    - Multichannel, high precision TDC
    - Mezzanine card support and readout
      - ADC front end
      - Additional optical links
      - …
- Part of a complex system as general purpose board

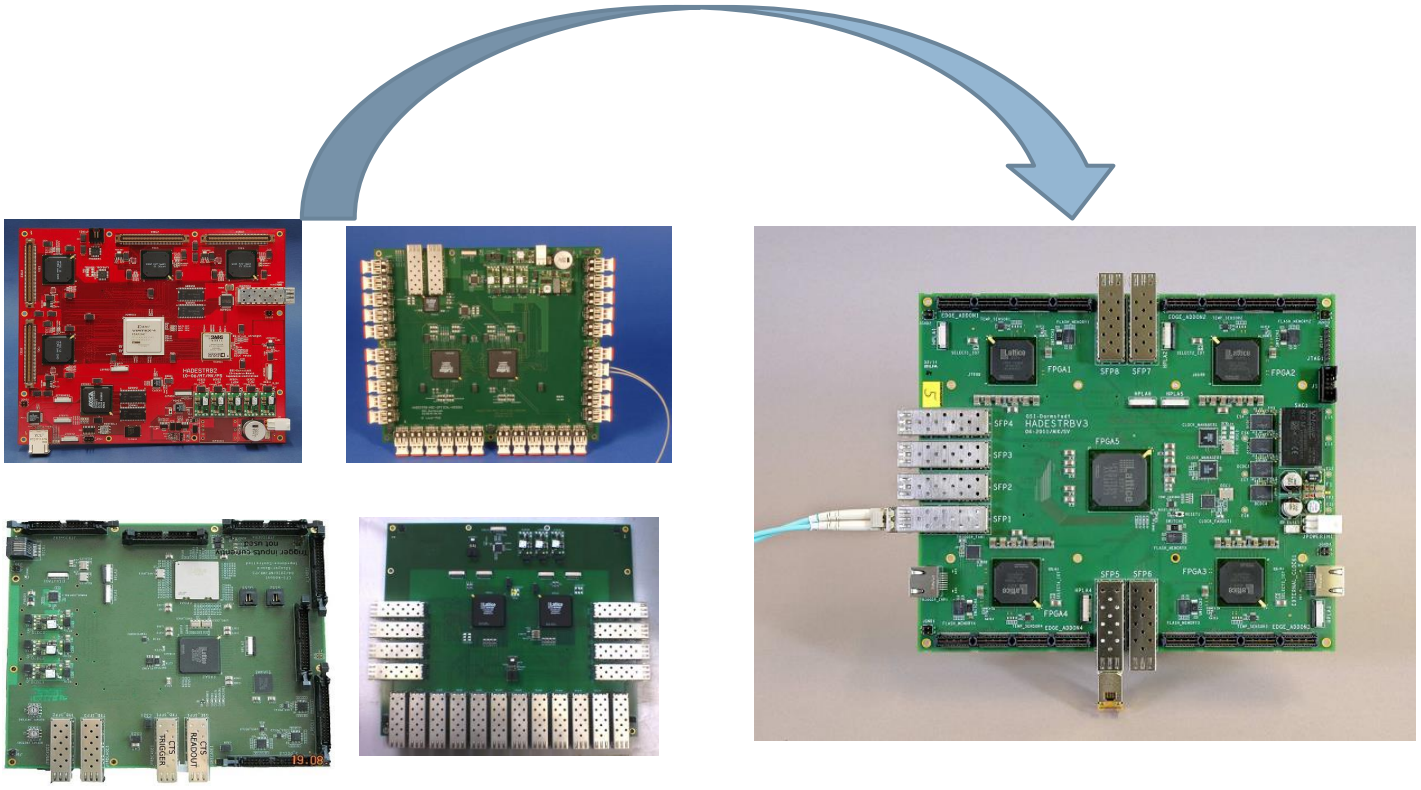


Trigger Readout Board v3



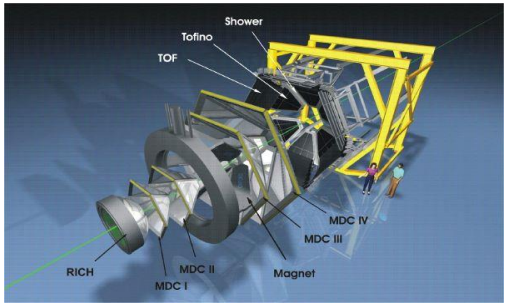


Trigger Readout Board v3

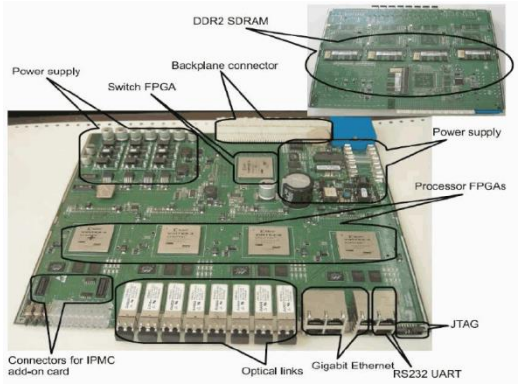


Main experiments

- HADES
  - Entire DAQ based on custom electronics equipped with FPGAs
    - 550 devices, 1050 transceivers, 80 000 channels
    - 55kHz event rate, 700MBps written to storage
  - Many successfull beamtimes



- PANDA
  - Electronics used to readout many prototypes
  - Main working horse – Compute Node
    - ATCA module
    - Data collection and event building on FPGAs



- PET prototype
  - High precision time measurement required
  - Triggerless readout
- More than 20 other clients for TRBv3

Summary

- Progress in technology introduces FPGAs as high performance and versatile devices
- Hardware developement pushed back by firmware developement
- TRBv3 as a perfect example of general purpose board