A novel method of measurement of time and amplitude of analog signals based solely on FPGA units

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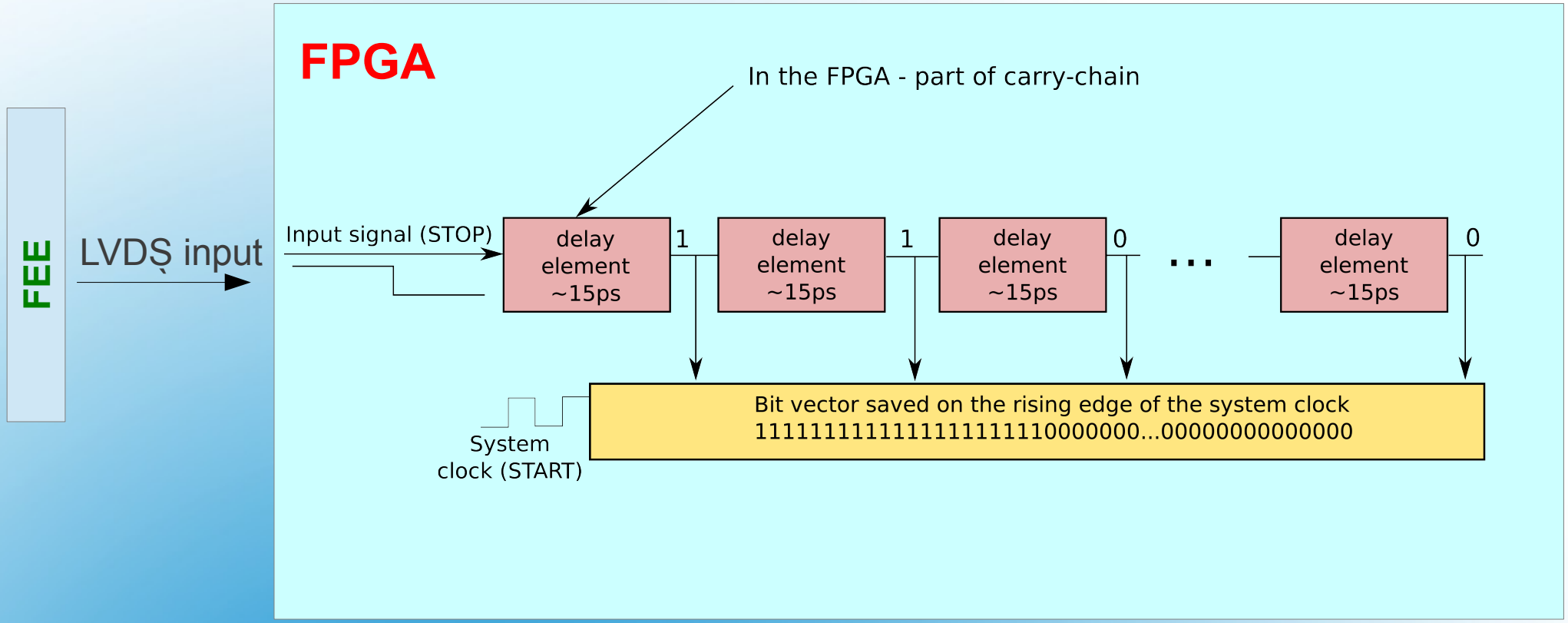
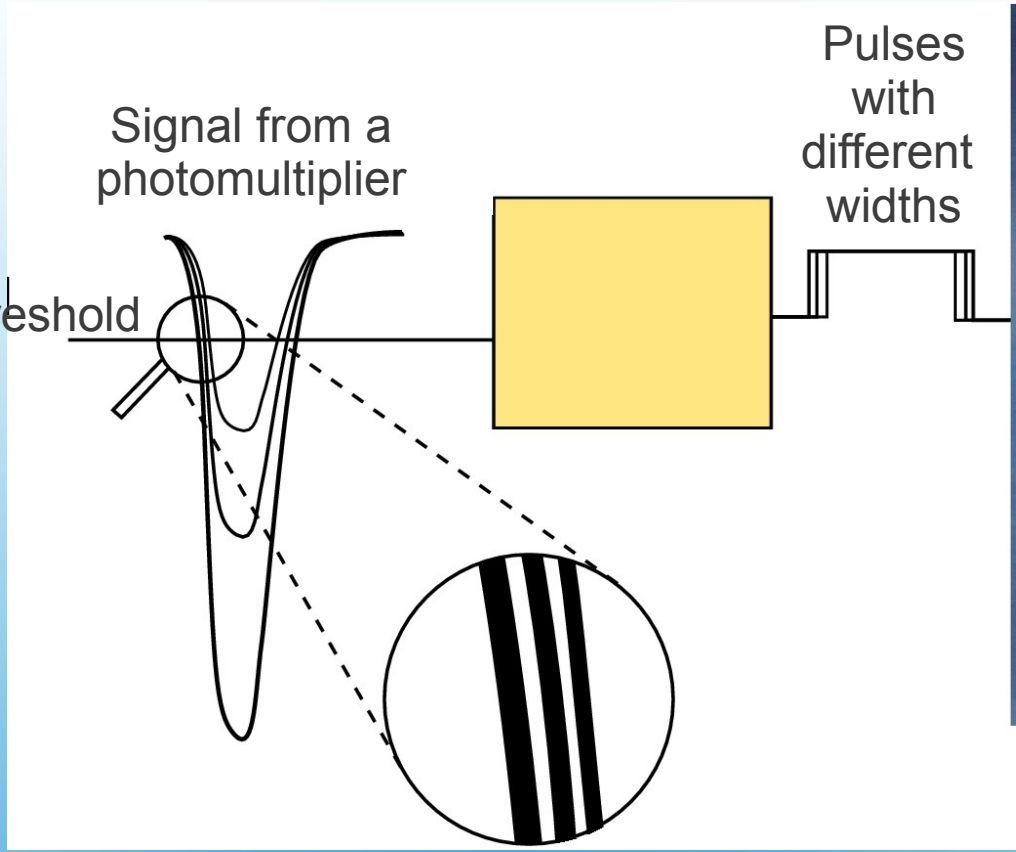
Requirements for the J-PET FEE

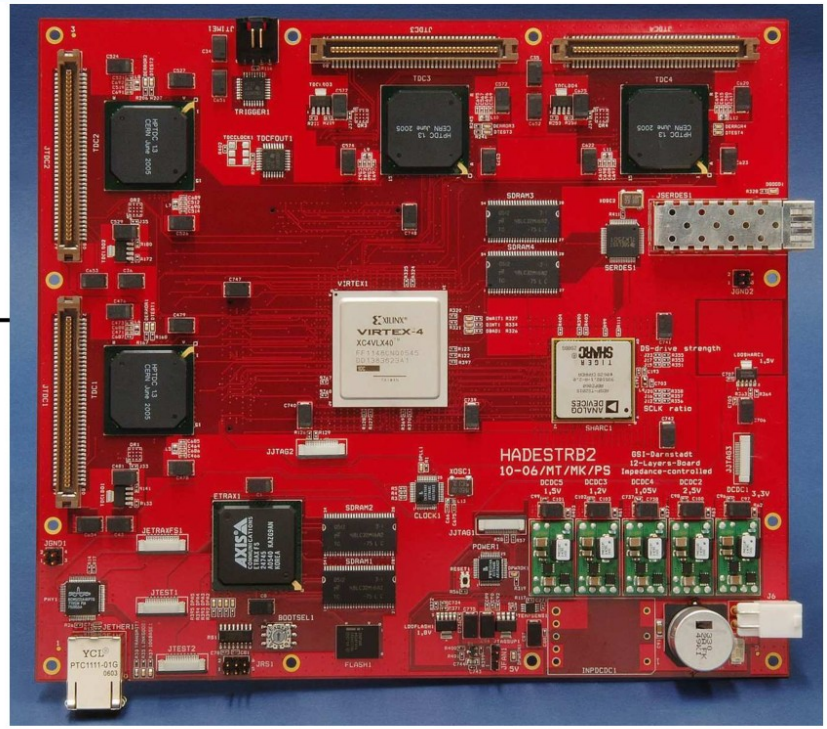
- Basic requirments for the front end electronics
  - Induced jitter as low as possible <20ps,
  - Measurment of negative signals up to 10V,
  - Possibility of charge measurment – discrmination of the signal (ToT) or charge to width circuit,
  - Signal preparation for TDC (time to digital converter) – discrimination of the signal.



C Ugur, E Bayer, N Kurz and M Traxler; „A 16 channel high resolution (<11 ps RMS) Time-to-Digital Converter in a Field Programmable Gate Array„; Topical Workshop on Electronics for Particle Physics 2011 (TWEPP-11)

FPGA-TDC



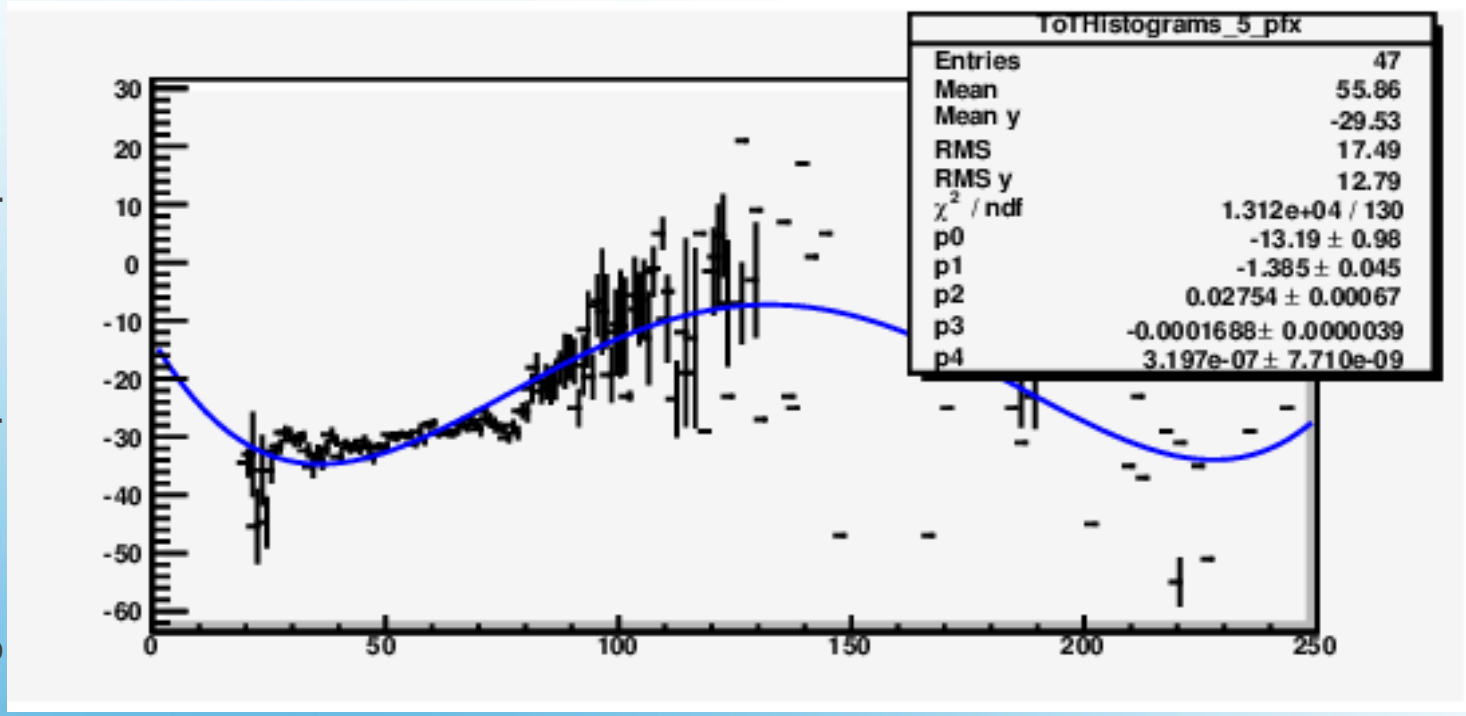


Measurment board

Time walk – can be compansated with charge to width corrections

Time over Threshold (ToT) or direct charge measurment

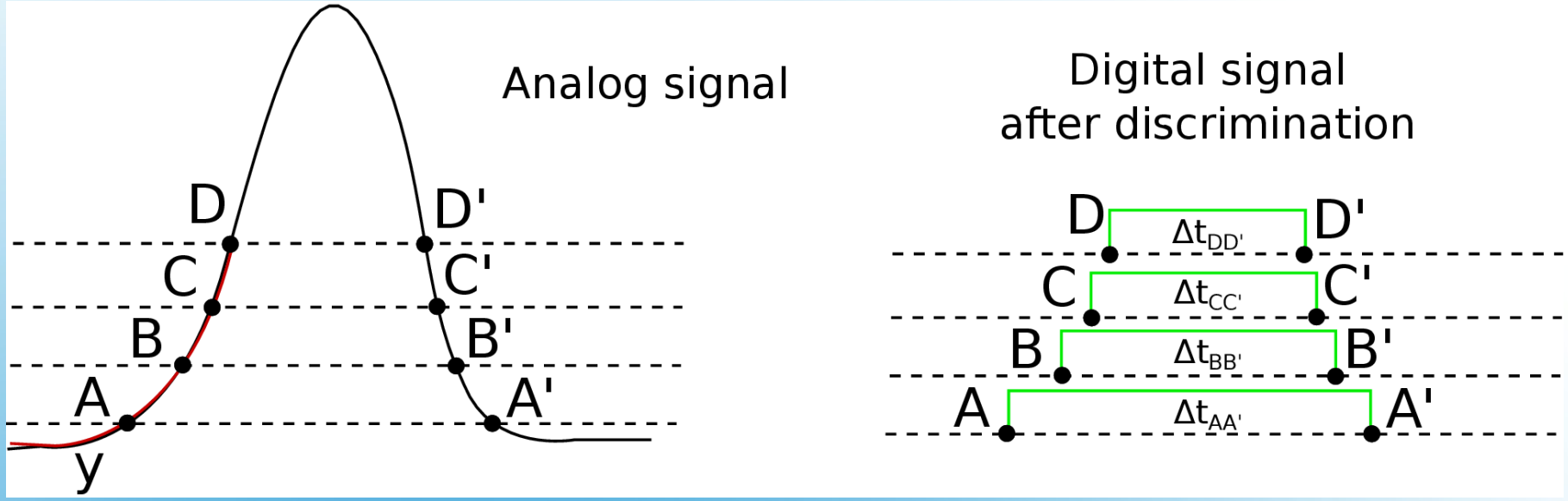
What are the intrinsic problems



Time walk – can be compansated with charge to width corrections

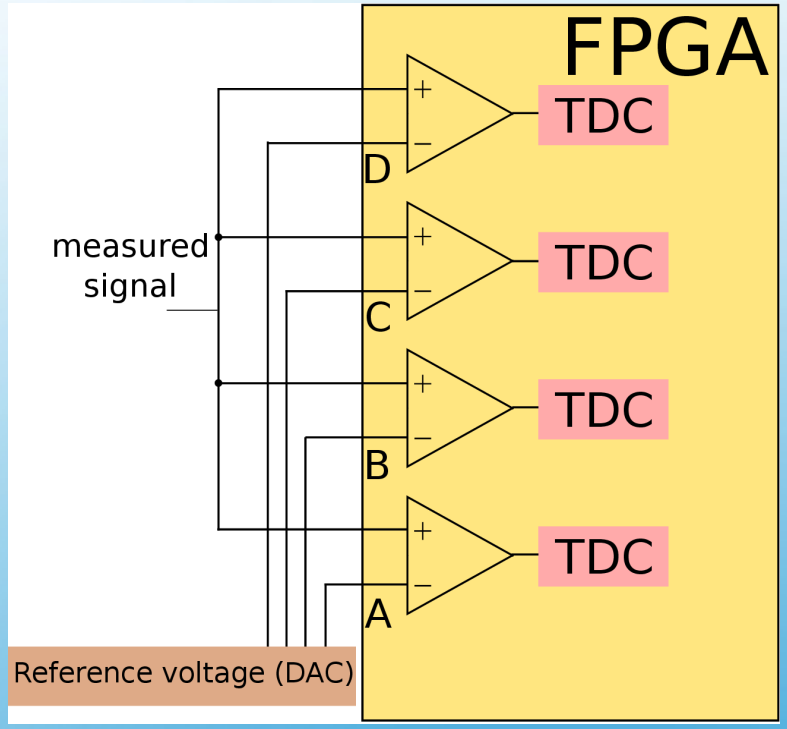
Time over Threshold (ToT) or direct charge measurment

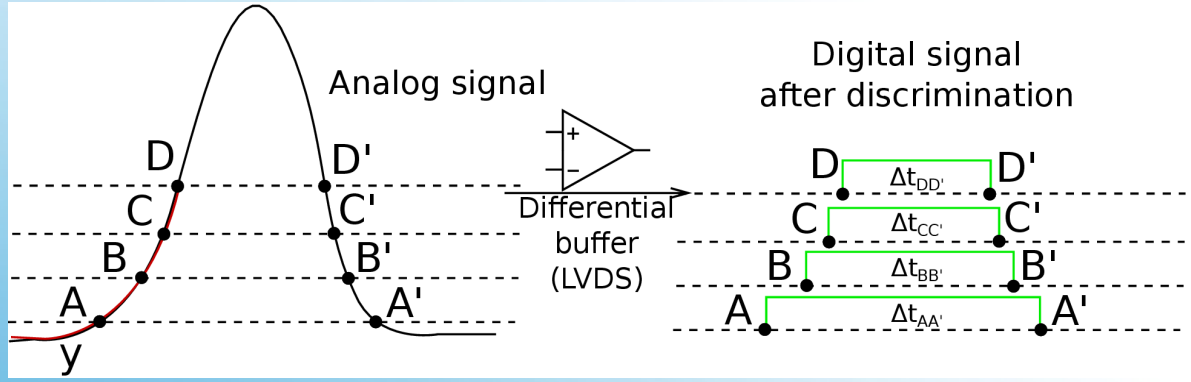
How to correct time measurments



Measuring with several thresholds and
fitting a curve to get start point (red line)
or charge (fitting full signal)

How to improve precision of time measurment

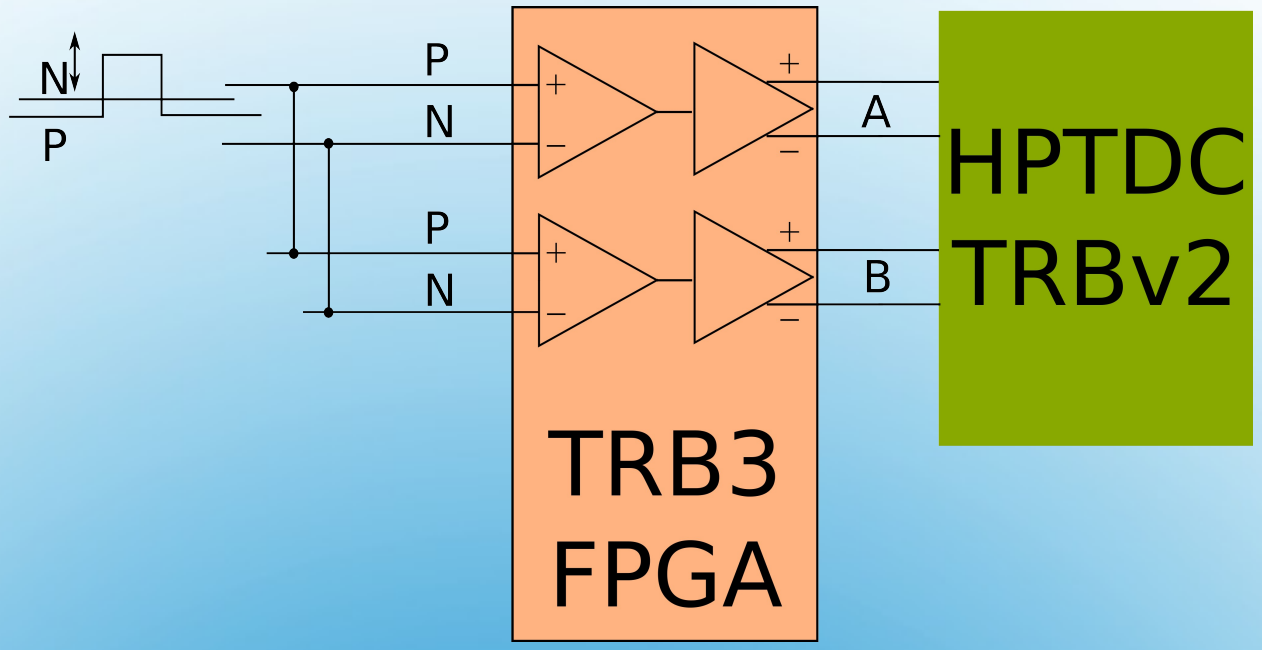




LVDS buffer is used for differential digital signals (P,N).
If P>N than it gives logical '1' otherwise '0'.

Why not to use it as a comparator ?

New front end – a mixture of digital and analog part

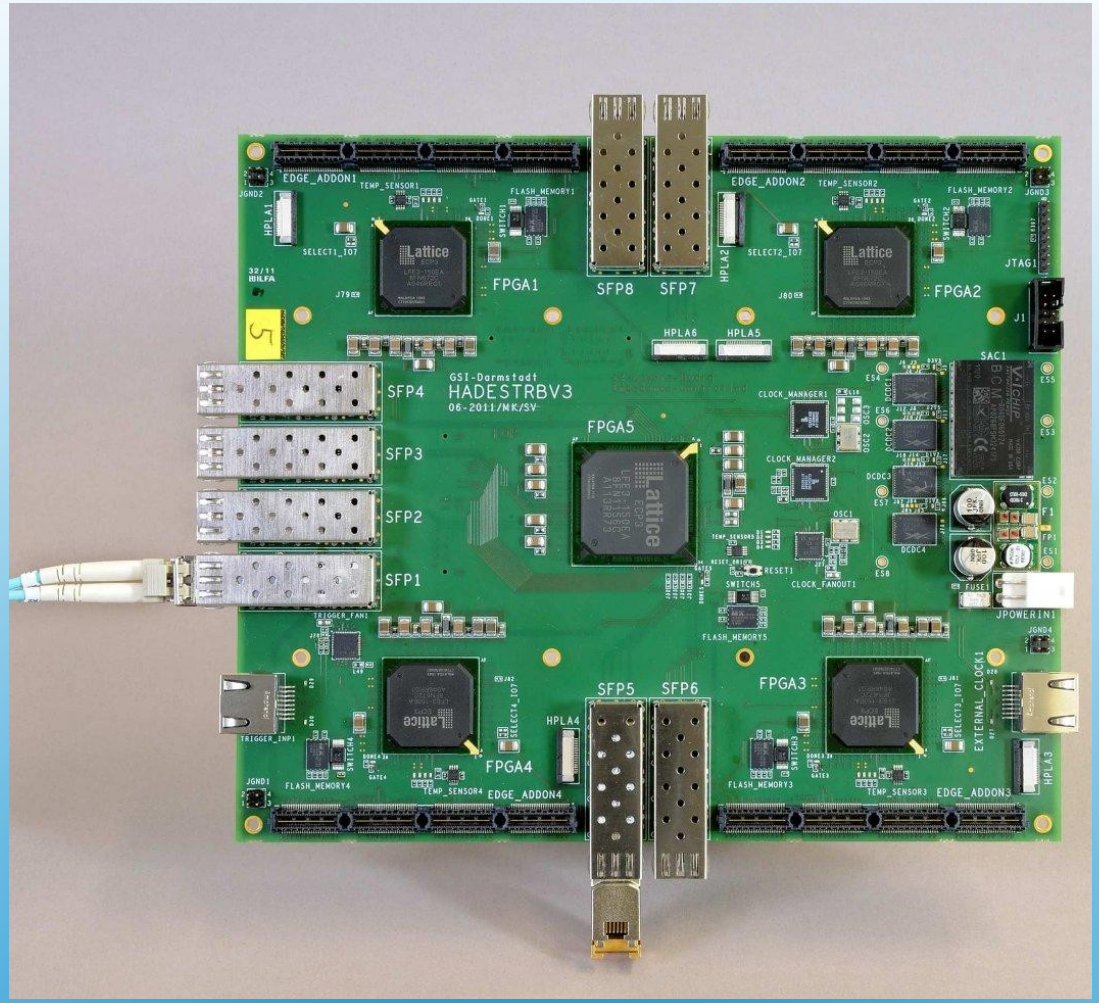


TRB – Trigger Readout Board.
TRBv2 – equipped with „traditional" TDC ASIC.

TRB3 can serve as FPGA-TDC – up to 256 chanels with 10ps resolution …
(here TRB3 FPGA-TDC is not used)

Channel res. (RMS)	Diff (P-N)
[ps]	[mV]
13	960
13	817
11	640
10	462
10	284
15	106
23	71
31	53
51	46
67	35
195	24
234	21

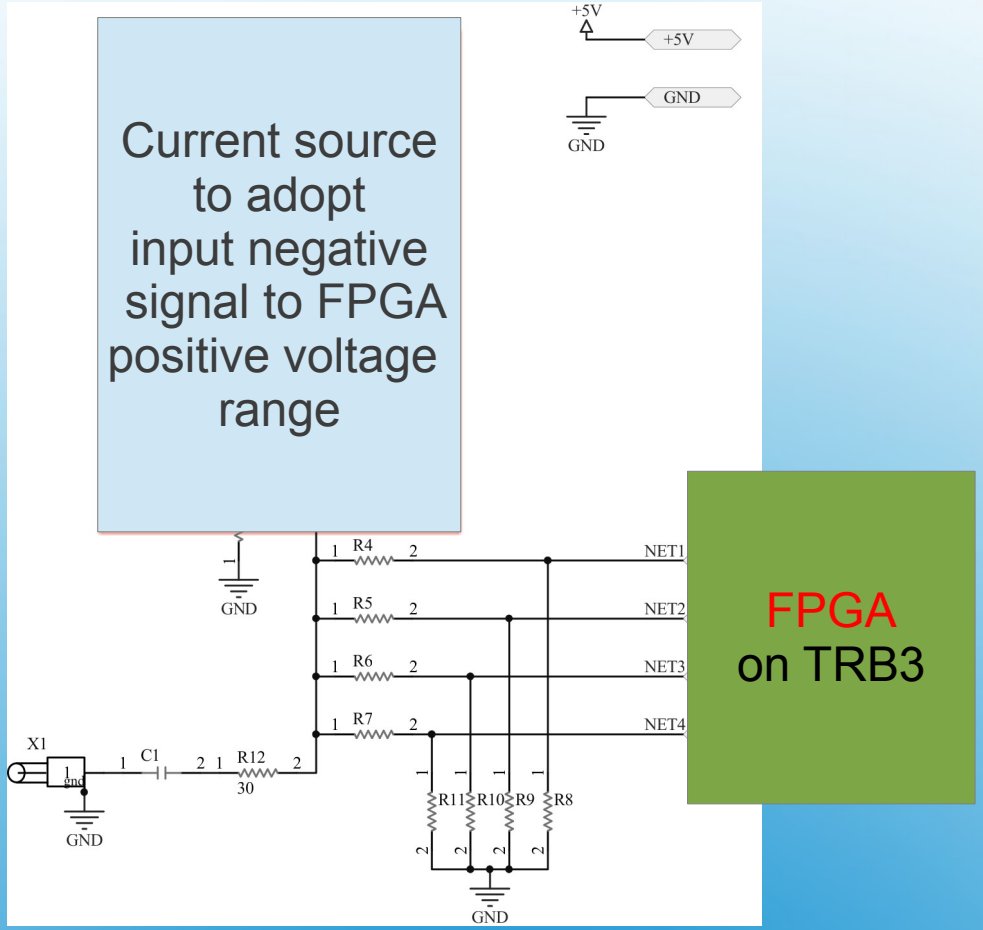
Checking LVDS buffer (just a beginning ...)

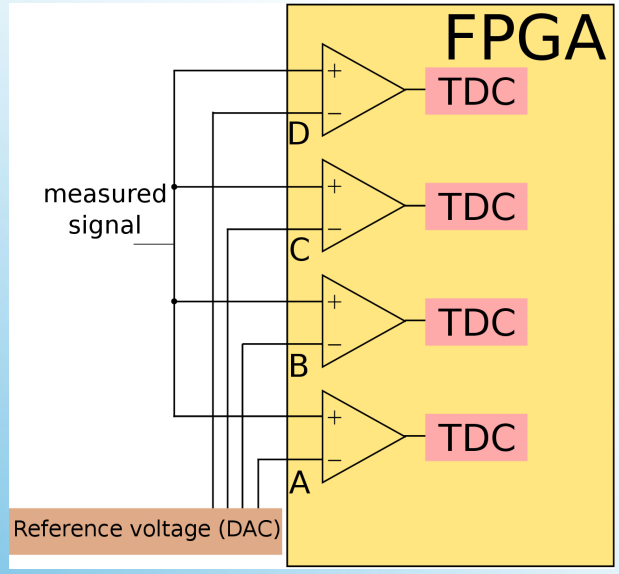


- Board produced and has all basic functionality (FPGA programming etc.)
- configuration loaded via network, data transfer implemented (G.Korcyl)
- TDC firmware provided – 256 high precision TDC channels (~10ps RMS) (C. Ugur)

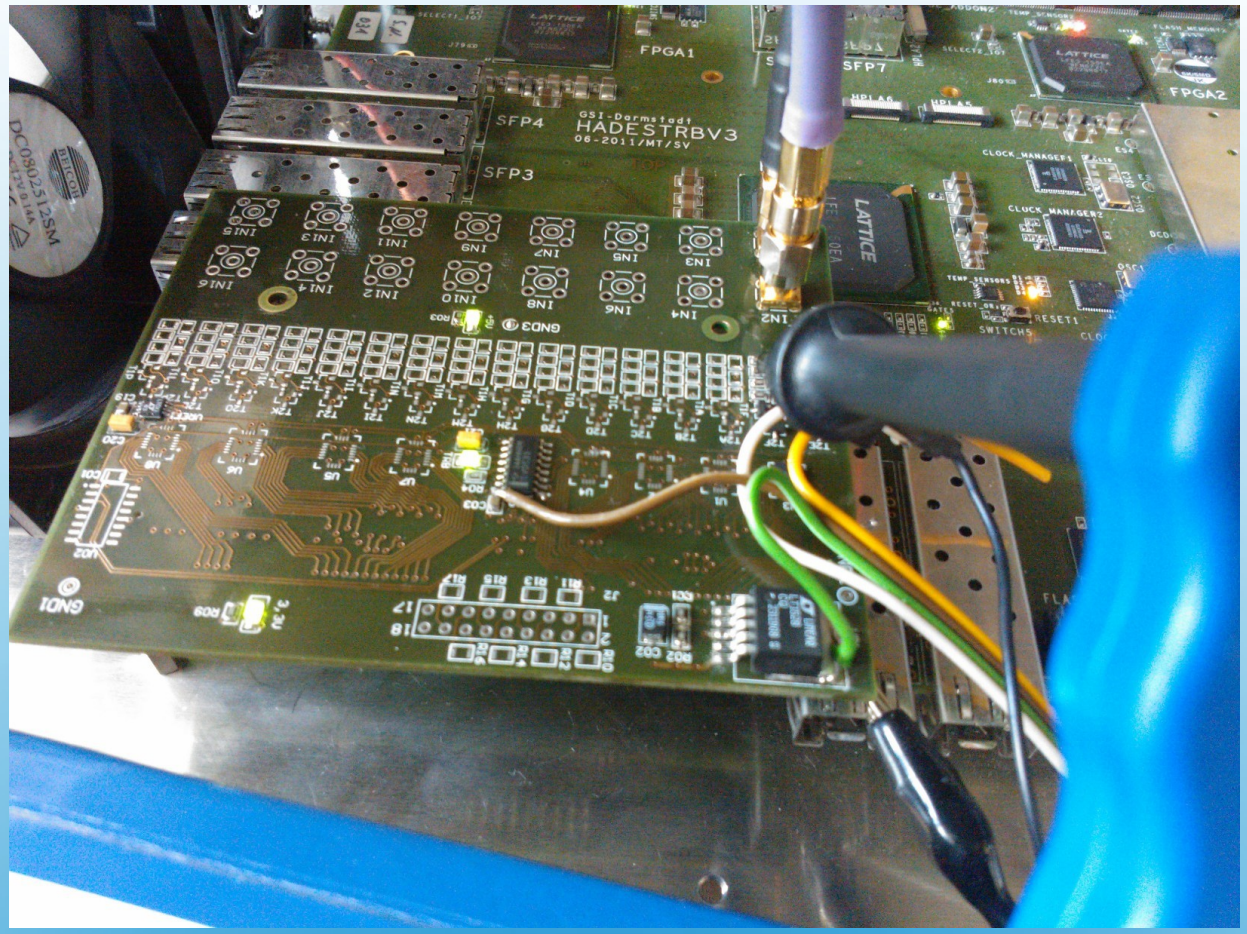
TRB3*

*"A compact system for high precision time measurements (< 14 ps RMS) and integrated data acquisition for a large number of channels" M Traxler, E Bayer, M Kajetanowicz, G Korcyl, L Maier, J Michel, M Palka and C Ugur, M Traxler et al 2011 JINST 6 C12004



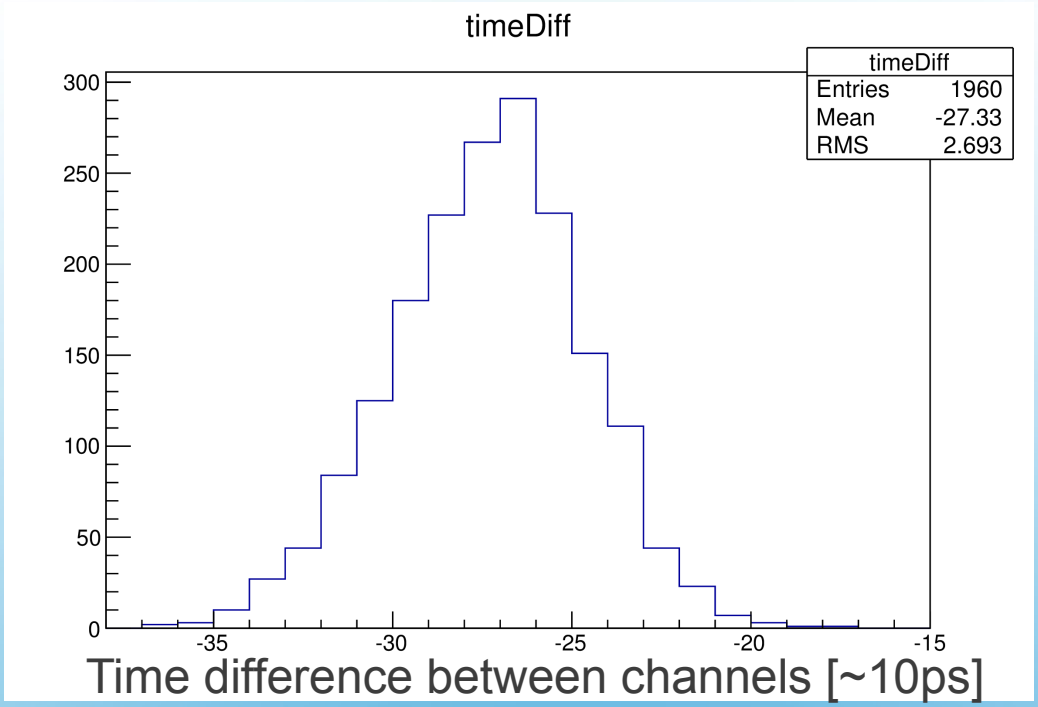


New front end – as simple as possible

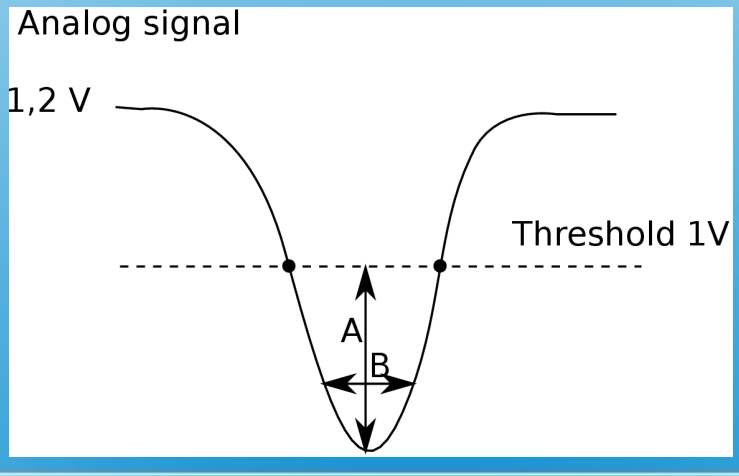


- 16 input channels
- Directly attached to the TRB3 (built at GSI Darmstadt, Germany)
- No need for external power supply - powered from TRB3
- Each splitted channel has high precision adjustable threshold
- Cost – 16 channels ~70EU
- Only two supply voltages (+3,+5V)
- ~1,5W per input channel
- small form factor

New front end - prototype



Built FEE induce only negligible jitter. (within some condions*) Measured for different threshold levels and fast signals (2ns width).



*Resolution depends on signal width (B) , difference between threshold and amplitude (A) and slopes

New front end – first results

- Prototype with 16 input channels has been built,
- First results are promising,
- There were bugs on the PCB board – new version is required (small changes)
- Amount of components should be reduced
- All functinality is functioning corectly (thresholds, precision ...)
- New PCB is ready for production
- More tests are required...

Summary & Outlook