TRIGGER-LESS AND RECONFIGURABLE DATA ACQUISITION SYSTEM FOR POSITRON EMISSION TOMOGRAPHY

Grzegorz Korcyl 2013

### **Detectors readout**



# Current electronics – Front End

- Front End Boards:
  - Fast, sharp input signals
  - Problem of "time walk"
  - KBv5
    - 4 input channels
    - For each:
      - Rise time fast measurement
      - Charge-to-Width measurement
        - Compensation of "time walk"
    - Custom format
  - KBv6
    - 2 input channels
    - For each:
      - Rise time fast measurement at 4 different levels
        - Offline shape recognition
    - Custom format
  - KBv7 (under development)
    - 3 input channels
    - For each:
      - Rise time fast measurement at 4 different levels
      - Charge-to-Width measurement
    - VME format



Time walk effect

- Some other FEE in development:
  - Marek's frontend
  - Mr. Majewski frontend
- Some other FEE from high energy physics experiments:
  - NINO board
  - PADIVA board

# **Current electronics**

- □ 5x Lattice ECP3 150 FPGAs
  - 4 edge devices
  - 1 central
  - Flash ROMs for each
- 8x 3.2Gbps optical links
- 4x 208pin QMS connectors
   Small Addons
- 1x 106pin connectorLarge Addon
- Hardware trigger input



TRBv2



TRBv3

# Reconfigurable electronics

- Programmable logic device
- Reconfigurable by the user
- Parallel processing
- Real-time processing
- Hardware features:
  - Memory blocks
  - Communication ports
  - Digital Signal Processing units
- □ CPU solutions (MircoBlaze, LatticeMico)
- SoC FPGA combined with CPU





# Reconfigurable electronics

Parallel - pipelined processing





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CPU

# Current Electronics - TRBv3

- Use of the internal structure of the chip to create delay chains
- Highly configurable TDC solution
  - Number of channels <-> single channel resolution
  - A lot of methods to improve resolution



# Current Electronics - TRBv3

#### Gigabit Ethernet link – Data Readout, Slow Control

- Full Duplex
- 118 MBps
- Basic protocols (IP, UDP, ARP, DHCP, ICMP, Custom)
- Autonegotiation + network address acquisition
- VLAN
- Jumbo frames
- Address filtering



Giagbit Ethernet with higher level protocols FPGA implementation

# **Current electronics - Triggering**

- Trigger board (in development) :
  - "Snapshot" of detectors status
  - "Triggerless system"
    - Periodic trigger signal
  - Optical connections
    - to each TRB
    - Trigger signal distribution
    - Event tag distribiution
    - Data readout
  - Data concentrator
    - Can perform online filtering/analysis



## **Current electronics**



## Prototype setup



# Software

#### Slow control

- Number of scripts to setup and start acquisition
  - Enclosed in GUI by Silvermedia
- Data collection event building
  - Standard event builder
  - DABC event building plugin
- Unpacking translation from HEX to meaningful format
  - Lightweight unpacker
  - GO4 module
  - Both produce ROOT tree structure
- Online monitoring
  - Histograms display in GUI by Silvermedia
  - GO4 GUI

# Software

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# Conclusions

- The entire readout chain is working and verified
- Hardware for the prototype:
  - TRBv3 is ready
  - FEE in development (previous versions under tests)
  - VME crate, fans, cables are being ordered
- Software for slow control
  - Basic scrips
  - Nice GUI under development
- Analysis software
  - 2 solutions:
    - Standard:
      - Event building verified
      - Lightweight unpacker verified
    - DABC and GO4:
      - Under verification