FPGA based data processing unit for J-PET data acquisition system

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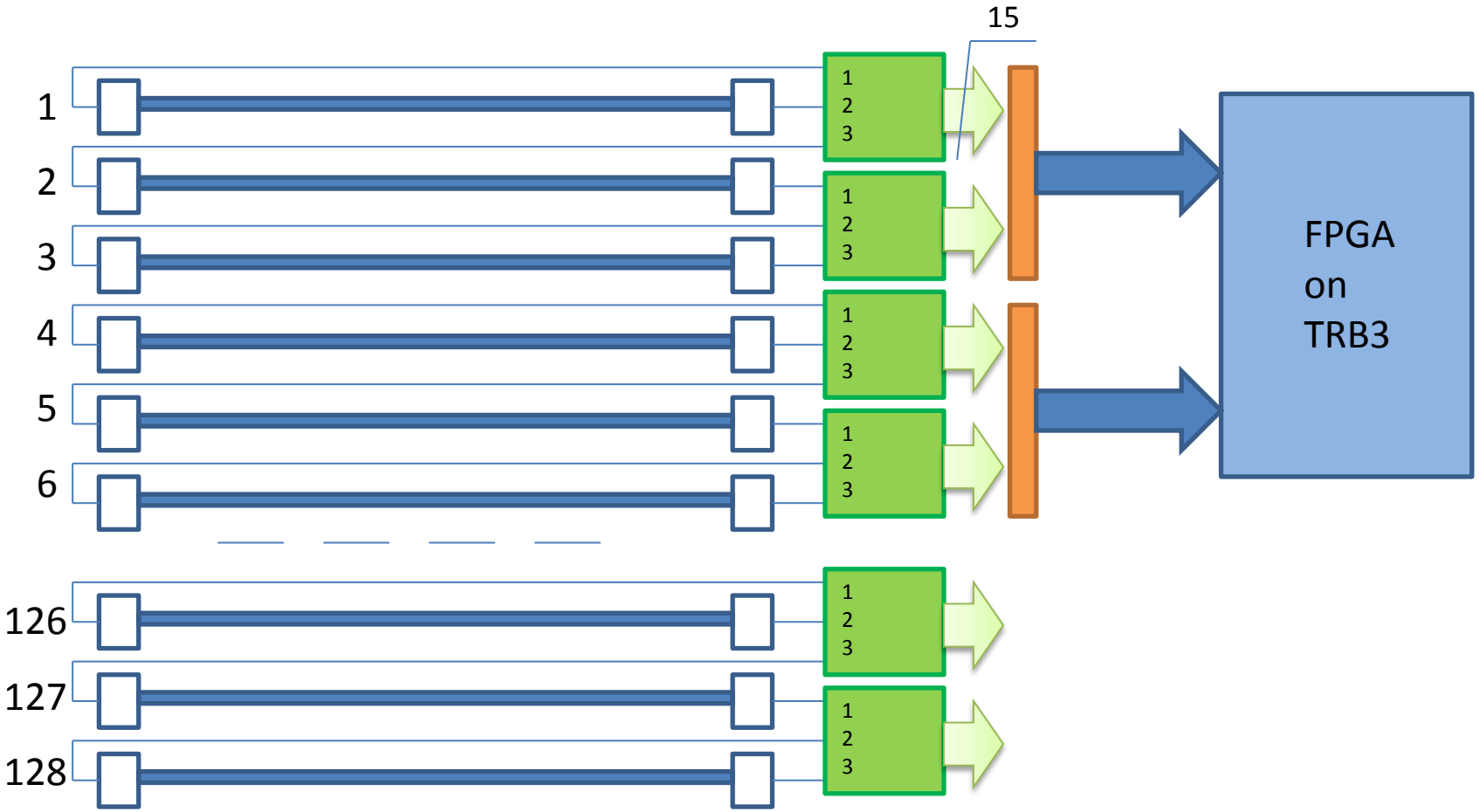
Addressed Issues

- Front-end arrangement
- Controller
- Zynq SoC FPGA
- Data transmission – rate, protocols
- Costs and timing
- PET Power Supply System

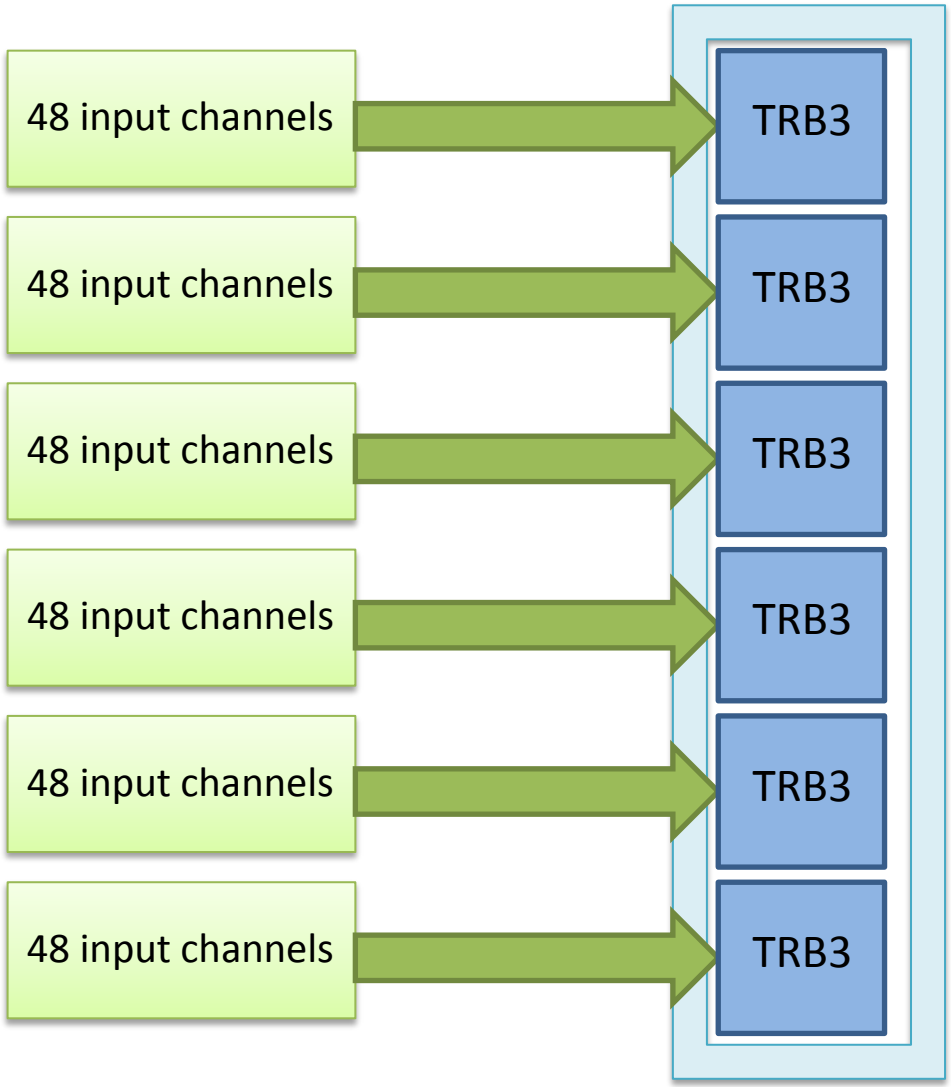
Read-out components

- 3-channel front-end card
- TRB3 card with 256-channel TDC on it
- Controller
- 19” crate
- Low Voltage Supply System
- High Voltage Supply System
- PC

Front End connections



Read-out crates



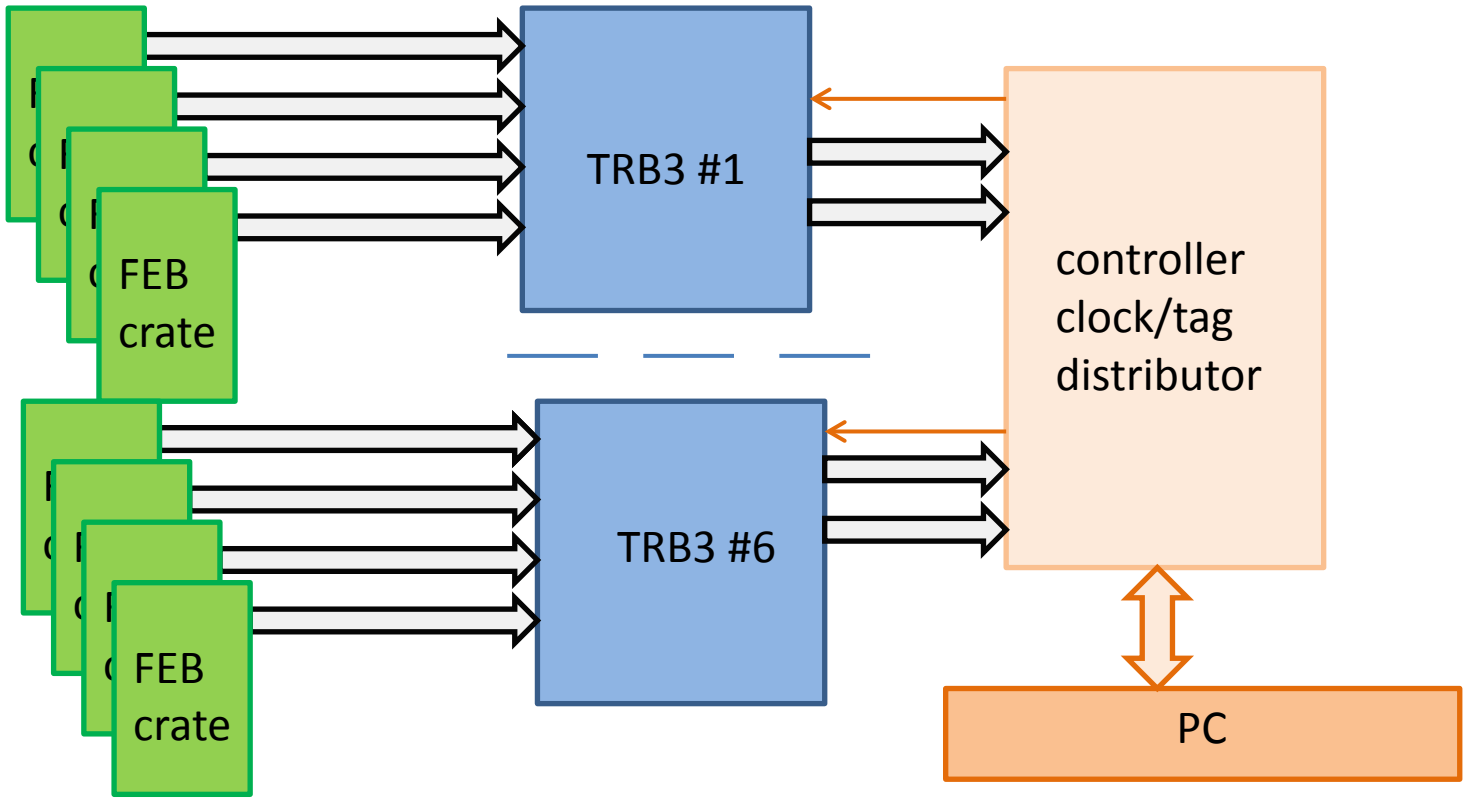
To handle 128 scintillators we need:

- Front-end cards: 86
- 19” crates: 6
- TRB3 boards: 6
- Controller: 1
- PC: 1

Max. number of front-end cards in 6 crates: 126

- Scintillators: 378
- TRB3 boards: 8
- Controller: 1
- PC: 1

Read-out System



Controller - clock/tag distributor

- Based on Zynq-7000 SoC
- 1 GB DDR3 SDRAM memory
- High volume memory on SD card
- 50 MHz clock source
- 12 - 16 clock outputs, LVDS
- Up to 15 serial fiber optic connections
- One or more Ethernet connections to PC

Zynq-7000 All Programmable SoC

FBGA package - number of pads: 900
28 nm, high-k metal gate (HKMG) process technology

- Processing System
- Programmable Logic
- Serial Transceivers
- PCI Express Block
- Two 12-Bit Analog-to-Digital Converters
- JTAG Boundary-Scan

Zynq Processing System

- Dual-core ARM® Cortex™-A9 Based Application Processor Unit
  - 2.5 DMIPS/MHz per CPU
  - CPU frequency: up to 1 GHz
  - ARMv7-A architecture
  - Single and double precision Vector Floating Point Unit
  - One global timer plus three watchdog timers
- Caches
  - 32 KB Level 1 instruction and data caches
    (independent for each CPU)
  - 512 KB 8-way set-associative Level 2 cache
    (shared between the CPUs)
- On-Chip Memory - boot ROM, 256 KB on-chip RAM
- 8-Channel DMA Controller

Zynq Programmable Logic

• Programmable Logic Cells:	478 000
• Look-up tables:	218 600
• Flip-flops:	437 200
• 36 Kb Block RAM [kB]	2 180
• DSP Slices (18*25 MACCs)	900
• Programmable I/O Blocks	492

Zynq – other features

- 16 Serial Transceivers
  - Supports up to 12.5 Gb/s data rates
- PCI Express Block
  - Supports Root complex and End Point configurations
  - Supports up to Gen2 speeds
  - Supports up to 8 lanes
- Two 12-Bit Analog-to-Digital Converters
  - On-chip voltage and temperature sensing
  - Up to 17 external differential input channels
  - 1 MSPS maximum conversion rate

PET System Data Volume

Assumption: 1 milion interactions per second

- 1 interaction generates 96 bytes of data
  - 4 PMT * 5 thr = 20 time values * 4 bytes = 80 bytes plus 16 bytes frame = 96 bytes
- 1 milion interactions * 96 bytes = 96 MB/s
- 6 TRB3 - > 96/6 = 16 MB/s from one TRB3
- 16 MB/s + 20 % overhead -> 19,2 MB/s
- Controller receives **115,2 MB/s** from six TRBs

Controller functions

- Clock distribution
- Event tag distribution
- Slow controll, alarm handling
- Data filtering/preprocessing -> volume compression

Protocols

- Front End settings – simple serial interface
- Front End to TDC inputs – LVDS
- Controller <–> TRB3: 8B/10B based custom point-to-point protocol
- Controller <–> PC: PCI Express or/and UDP/IP
- Controller <–> HV and LV PS: RS232 or RS485

Prototype Component Costs estimation

- Zynq FPGA (1pc): 10 000
- SFP (10 pcs): 2 500
- Other Ics: 2 500
- PCB prototype: 4 500
- Assembling: 2 500

total: **22 000 PLN**

Time schedule

- Now: schematic design in progress
- Expected end of design: X.2013
- Design of PCB: XI.2013 - II.2014
- Assembling: III.2014
- Board ready for tests: IV.2014

Some points to be solved:

- Mechanical standard for TRBs and PC
- Software development:
  - VHDL code developmnent
  - ARM programming
  - PCI Express

PET Supply System

Supply Voltages Needed:

- ± 5 V - front end boards
- +12 V - front end boards, input part
- +48 V - TRB boards
- -2500 V - photomultipliers

Current Consumption Estimation

Final configuration: 128 scintillators –> 256 PMTs

		one channel	total	power
• +5 V	-	700 mA	180 A	900 W
• - 5 V	-	200 mA	52 A	260 W
• +12 V	-	500 mA	128 A	1536 W
• +48 V	-	400 mA	2.8 A	135 W
		Total Power:		**2.83 kW**
• -2500 V	-	100 µA	26mA	65 W

Complete Supply System

- Low voltages (Wiener, Plein & Baus GmbH):
  - PL506 + PBX506-EX 3 kW main low voltage supply crate
  - MEH02/07 for ±5 V – maximum 115 A **3** modules
  - MEH07/16 for +12 V – maximum 46 A **3** modules
  - MEH30/60 for +48 V – maximum 13.5 A **1** module
- High voltage (Caen, S.p.A.):
  - SY4527B main high voltage supply crate
  - A1536N – 32-ch module – max. -3 kV, 1 mA **8** modules

Current PS Status

- Low voltages
  - PL506 + PBX506-EX 3 kW main PS — 1 crate
  - MEH02/07 for **±5 V** – maximum 115 A — 2 modules
  - MEH07/16 for **+12 V** – maximum 46 A — 1 module

    2 more modules to be bought
  - MEH30/60 for **+48 V** – maximum 13.5 A — 1 module
- High voltage
  - SY4527B - 600 W main PS — 1 crate
  - A1535SN – 24-ch (-3.5 kV, 3 mA) — 2 modules

    7 or 8 more modules to be bought

Mechanics

- 19” crates in racks:
  - Front-end: 86 3-channel boards -> 6 crates

    One 19” crate for front-end bought (covers 48 channels)
  - TRB: 256-channel TDC -> 6 TRBs -> 1 crate (?)
  - Low voltage Power Supply -> 2 crates
  - High voltage Power Supply -> 1 crate

We need two racks.